THREE DIMENSIONAL INTEGRATION AND ON-WAFER PACKAGING FOR HETEROGENEOUS WAFER-SCALE CIRCUIT ARCHITECTURES

Linda Katehi, Barry Perlman[1], William Chappell[2], Saeed Mohammadi[2] and Michael Steer[3]

University of Illinois, Urbana-Champaign, IL, Katehi@uiuc.edu

[1]CERDEC, US Army RDECOM, Ft. Monmouth, NJ, Barry.Perlman@us.army.mil

[2] Purdue University, West Lafayette, IN

[3] North Caroline State University, NC

I. INTRODUCTION

Advanced Network Centric Warfare (NCW) systems are critical to the successful implementation of the Army's Future Force. These systems require a new generation of circuits with deployable, agile, versatile, lethal, survivable and sustainable capabilities. Both manned and unmanned vehicles are required to established dominance in the battlefield via use of multi-band, agile, multifunctional mobile systems that can control, command and communicate. However, at very high frequencies and with wide analog and digital bandwidths, conventional chip-substrate integration techniques and filtering technologies (e.g. solder bumps and wire-bonds) such as the ones mentioned above, limit system capability and compromise efficiency.

The super-heterodyne radio architecture, most prevalent in present systems, necessitates multiple passive off-chip components including IF filters adapted to the channel filtering requirements to support different standards. A newer direct conversion (including low IF) architecture has evolved that lends itself to a single- or few-chip mixed signal implementation although performance is compromised primarily because of the loss and finite Q of on-chip passives leading to low RF efficiency, increased power consumption and high phase noise. In this circuit architecture, digital noise is coupled into the RF circuitry further limiting detectability. For future NCW systems, the above attributes must be obtained with performance superior to that available commercially and delivered with volumes

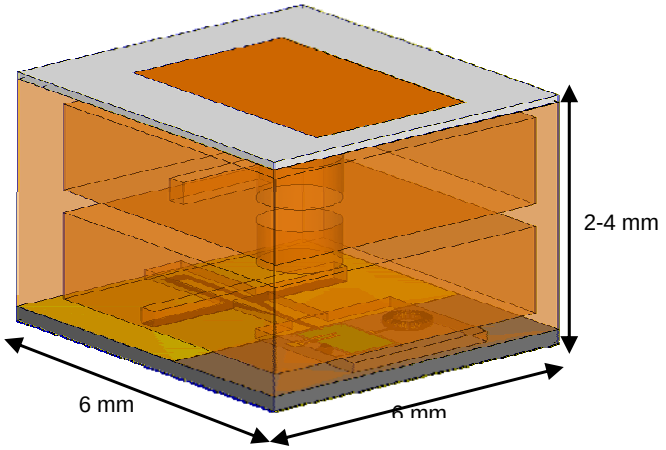

Figure 1: Multi-wafer Three-Dimensional Integration

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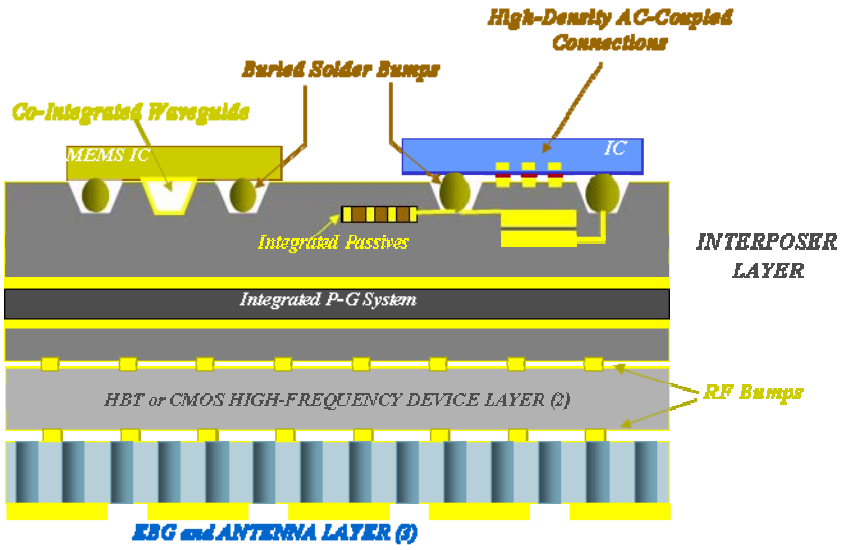

Figure 2: Highly Integrated Advanced Transceiver Module

relatively small in comparison to that in the commercial world.

These performance requirements put a put a premium on heterogeneous integration whereby various optimized chip and component technologies can be combined to obtain superior overall performance. For example, combining the high power of a high-resistivity SiGe power amplifier chip with the wide operating frequency range and compactness of a CMOS mixed signal chip operating with 1.2 V supply, provides circuits with the density of flash memory and with the agility afforded by the evolving technologies of ferroelectrics and MEMS actuators.

Our experience of the past ten years has shown that the requirement of good performance, low cost and high operating frequencies cannot be achieved either by monolithic or hybrid integration. It is the synergistic development of technologies and RF architectures that will enable us to achieve superior performance while constraining costs and achieving multi-functionality and agility. Three-dimensional integration and on wafer packaging of

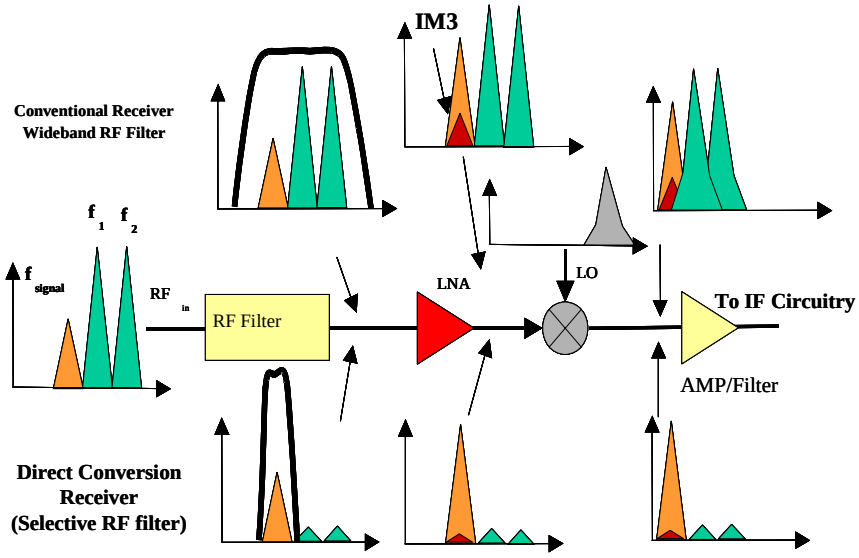

Figure 3: Comparison of Conventional and Direct Conversion Receiver Architectures

heterogeneous wafers (see Figure 1) is the future in high frequency circuit design and circuit architecture. It leads to the development of novel RF front-end transceiver architectures that consume very little power, are highly compact, very low-cost and high-performance and are appropriate for future NCW systems.

To achieve high performance the passives are required to exhibit high Q, small size and low cost. It is known that on chip passives suffer from low Q while off-chip components are not easy to integrate with the active chips. A new concept introduced recently, ***the use of a high-frequency interposer layer***, allows for the combination of high-performance, low cost and the ability to integrate in three dimensions. The use of an interposer layer (see Figure 2) that can tightly integrate active chips with passives in a multi-wafer environment also provides multi-functionality due to the ability to integrate with high and intermediate permittivity dielectrics (relative permittivity of 600 and 25 respectively). The use of these dielectrics on the interposer leads low parasitics, high density and low cost. The interposer can incorporate heterogeneous materials for more functionality. As an example, ferroelectric components using BST (Barium Strontium Titanate) and designs that exploit their tunable characteristics have been developed. The BST has been integrated into the interposer using a heterogeneous integration method.

The potential of using high density, low-loss interconnects and integrated high quality passives, in order to complement the advances in high speed device technology, has been shown to provide maximum benefit for integrated microwave systems. Both design cycle times and system performance have been advanced through the use of high-resistivity silicon in a unique Si-based Self-Aligned Wafer Level Integration Technology (SAWLIT), that was developed as part of this project. In this technology the CMOS or SiGe ICs are integrated within the Si interposer using low-loss interconnects with a definition better than 1 micron. This integration approach allows the removal of passives from the expensive IC chip and their integration on the interposer for lower cost and better performance. Additionally, the use of a multi-layer package integrated with the interposer allows for the high density integration of high quality components such as cavity based filter with unloaded Q's > 1500s.

In this paper we will present the implementation of the interposer concept on a transceiver architecture that easily lends itself to a three-dimensional heterogeneous integration along with the passives that make this integration possible [7-9]. The three-dimensional circuit architecture will be demonstrated on a 10GHz CMOS receiver.

II. TRANCEIVER ARCHITECTURE

Herein, we present a futuristic three-dimensional transceiver architecture which utilizes a high-Q integrated filter and relies on vertical integration for the development of a compact three-dimensional wireless front end. This system has an antenna structure intimately integrated with the highly selective multi-frequency substrate and incorporates a novel mixed signal digital IF circuitry including integration of the ICs with the mixed signal circuitry ***through a uniquely designed Si interposer layer***. The design of this transceiver can be accomplished effectively through a holistic mixed circuit approach that accurately takes into account high frequency effects including dispersion, radiation and electromagnetic coupling. This transceiver has the potential to outperform many existing systems such as JTRS and SATCOM. Further it demonstrates the potential of many novel circuit technologies to provide the functionality and density needed in systems such as Cognitive Radio, the next generation sensors, etc.

This three-dimensional architecture promises compatibility with multiple standards for multifunction, high-density of integration for very small volume and lower fabrication cost, and low power consumption. Some of the important aspects of this architecture are RF compatible packaging, low-frequency IF, all-Si based circuit realization for up to Ka-band frequency, relaxed

specifications on linearity, dynamic range, image frequency rejection, phase noise and digital IF down-conversion, filtering, demodulation and signal processing [1]-[5].

Good transceiver performance critically depends on the ability to integrate on wafer heterogeneous materials, technologies and high-Q embedded passives with the active chips. Cost reduction is a major reason for the use of the interposer concept. The ability to integrate a very high Q filter with the LNA, VCO and antenna allows for a direct conversion as shown in the schematic of Figure 3.

Direct conversion receivers are very sensitive to LO leakage, DC offset and baseband noise sources, which cause severe performance degradation compared to super-heterodyne architectures. The ability to integrate a high-Q filter allows for the use of a low IF frequency selected close to the baseband, above the 1/f noise corner frequency, but still low enough for direct A/D conversion. With good RF channel selectivity, system specifications such as the linearity of the low noise amplifier (LNA), the phase noise of the voltage-controlled oscillator (VCO), the image frequency rejection requirement and the dynamic range of the A/D converter can be substantially relaxed (Figure 3). The value of the IF that can be utilized in this architecture critically depends on the characteristics of the receiver including the quality factor of the RF filters. Traditional analog signal processing such as I and Q separation (In-phase and Quadrature-phase), channel-select filtering, down-conversion to baseband frequency and moving target indication (MTI) can be moved into the digital domain, thereby avoiding the sensitivity of this process to various analog circuit impairments and providing adaptation to the multiplicity of standards and multifunctional capability.

The receiver architecture of Figure 3 requires a number of novel technologies which have been developed and are described below. These technologies, when applied to transceiver designs can lead to state of the art system architectures with unparalleled performance. A detailed description of the development effort for each of these novel technologies is described in the following sections.

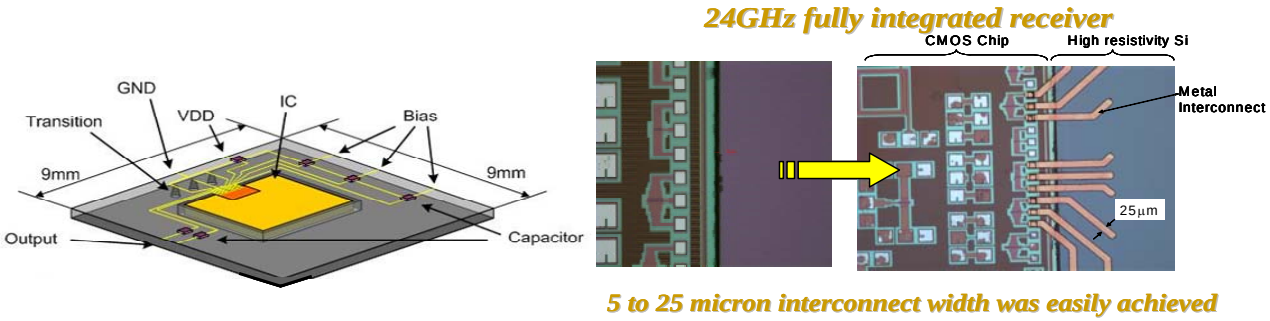

Figure 4: Si-based Self-Aligned Wafer Level Integration Technology (SAWLIT) for a Si Interposer

III. HETEROGENEOUS INTEGRATION AND THE CONCEPT OF INTERPOSER

To achieve high performance in the transceiver architecture of Figure 3, the passives are required to exhibit high Q, small size and low cost. It is known that on chip passives suffer from low Q while off-chip components are occupying a large volume and are not easy to integrate with the active chips. A new concept introduced recently, ***the use of a high-frequency interposer layer***, see Figures 1 and 2, allows for the combination of high-performance, low cost and the ability to integrate in three dimensions. The use of an interposer layer, as shown in Figure 2, that can tightly integrate active chips with passives in a multi-wafer environment also provides multi-

functionality due to the ability to integrate with high and intermediate permittivity dielectrics (relative permittivity of 600 and 25 respectively). The use of these dielectrics on the interposer leads to low parasitics, high density and low cost in addition to providing more functionality. As an example, ferroelectric components using BST (Barium Strontium Titanate) and designs that exploit their tunable characteristics have been developed. The BST has been integrated into the interposer using a heterogeneous integration method [10].

The integration of heterogeneous layers may compromise reliability as operating power increases due to thermal mismatch issues. In this case distributed cooling will be required to provide better control of the thermal environment. The use of passive or active cooling via use of three-dimensional cooling channels is compatible with the three-dimensional technology presented herein. Integrated cooling is a growing research area in high-frequency circuit design.

Through DARPA's TEAM project led by Purdue University and North Carolina State University we have demonstrated the use of interposer integration and packaging techniques using high frequency CMOS and SiGe circuits. The potential of using high density, low-loss interconnects and integrated high quality passives, in order to complement the advances in high speed device technology, has been shown to provide maximum benefit for integrated microwave systems. Both design cycle times and system performance have been advanced through the use of high-resistivity silicon in a unique Si-based Self-Aligned Wafer Level Integration Technology (SAWLIT) [6], see Figure 4, that was developed as part of this project. In this technology the CMOS or SiGe ICs are integrated within the Si interposer using low-loss interconnects with a definition better than a few microns. This integration approach allows the removal of passives from the expensive IC chip and their integration on the interposer for lower cost and better performance. Additionally, the use of a multi-layer package integrated with the interposer allows for the high density integration of high quality components such as cavity based filter with unloaded Q's > 1500s.

High-valued components such as decoupling capacitors or choke inductors, high-Q components with quality factors greater than 100, or tunable components which require precise fabrication

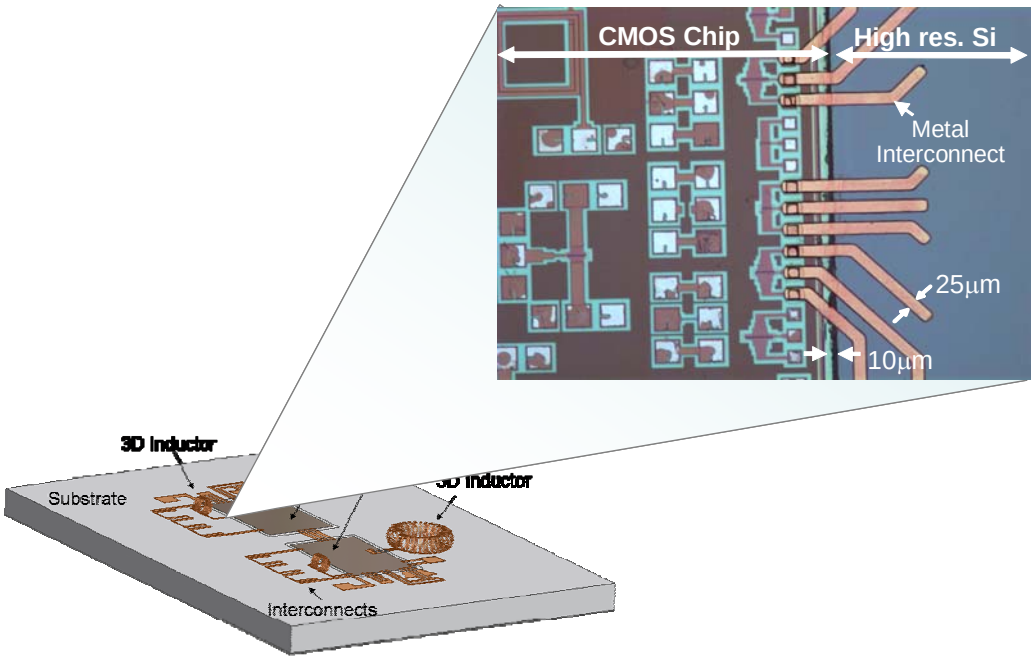

Figure 5: Interposer integration for a wireless transceiver system. A CMOS chip is integrated inside a high resistivity Si. Interconnects as narrow as 25μm are used

conditions not compatible with CMOS fabrication lines cannot be integrated into a single piece of silicon despite the advances of high frequency transistors.

Through the use of a silicon interposer as a heterogeneous integration platform, each of these components can be added to a mixed-signal System on a Chip (SOC) design providing improved performance in fully integrated systems. Additionally, the use of high quality passives in an interposer, which are in close proximity to the circuit through high density interconnects, allows for circuit rework without altering the expensive mask set needed for the CMOS/SiGe components, greatly reducing circuit design cycle and cost.

By developing novel three-dimensional integration schemes, we have demonstrated, for a first time, a fully integrated Si receiver at 10GHz using a Si-based interposer. Using SAWLIT [6,11], the 10GHz receiver designed in 180nm CMOS technology has been integrated with an embedded Si-based matching network, BST bypass capacitors and an integrated high-Q filter. The overall receiver system performance has been characterized, showing substantial improvement over other fully integrated systems operating at the same frequency and with similar bandwidth. Due to its inherent self-aligned characteristics, this technology allows for batch integration of multiple chips and is key to developing low cost and high performance fully integrated RF circuits and systems.

The high-Q filter for the receiver of Figure 2 is a three-dimensional structure that has been designed to provide high Q along with small size and the ability to become fully integrated with the interposer. In this arrangement, using the interposer as an integration platform, cavities within a Si wafer or a multilayer polymer materials have been fabricated to provide a multipole filter performance. For the polymer material, a three-dimensional laser fabrication method has been utilized to create evanescent filters with unprecedented quality factors Q greater than 1,000.

The multi-wafer architecture discussed above, shown in Figures 1 and 2, comprises three main structural and functional layers: the ***Interposer Layer (1)*** the ***HBT/CMOS Device Layer (2)*** and the ***EBG/Filtering and Antenna Layer (3).*** These layers are shown on the schematic of Figure 2. In this architecture the various ICs are bonded using SAWLIT to the multi-layered *interposer layer* which incorporates high-performance integrated passives and RF routing and is then integrated with a high-Q filter using Si or Polymer. Alternatively it can be integrated with an *Electromagnetic Band-Gap (EBG) Layer* and *Antenna Layer* for high-Q filtering and high-efficiency radiation.

An IBM 0.18μm CMOS technology has been used for the implementation of the low-power RF. In the following we will present the implementation of the interposer concept on a transceiver architecture that easily lends itself to a three-dimensional heterogeneous integration along with the passives that make this integration possible. The three-dimensional circuit architecture is demonstrated on a 10GHz CMOS receiver.

IV. 10 GHz CMOS INTEGRATED RECEIVER

Using the concepts developed above, a 10GHz CMOS receiver was designed and fabricated. The CMOS chip was fabricated on 7RF and was designed to operate at 10 GHz. The amplifier was tuned using a matching network printed on the interposer as shown on Figure 5. Using high Q passives on the low loss high resistivity Si Interposer, the input matching of the amplifier was improved from 13dB at 11 GHz to -30dB at the design frequency (10.2GHz). This improved matching increased the convergence gain of the receiver from 21 dB to 23 dB as shown on Figure 6. In this initial design the conversion gain at the center frequency was about 7 dB (about 2 dB higher than anticipated due to additional losses introduced by the coupling to the filter. At present design changes are implemented which are expected to reduce the Noise Figure to almost 5.5 dB at 10 GHz.

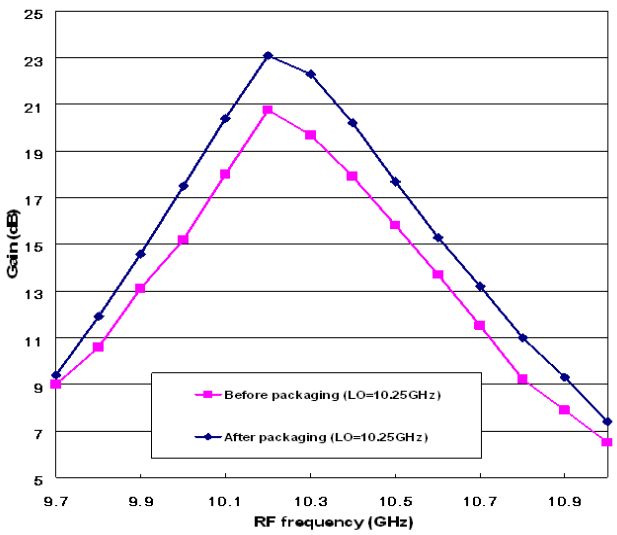

Figure 6: Convergence Gain of the 10GHz RFIC Before and after Adding the Embedded

V. CONCLUSIONS

This paper has presented circuit architectures which allow for the three-dimensional integration and on-wafer packaging through the concept of a Si interposer. The presented three-dimensional integration schemes have allowed for the design and fabrication of fully integrated receiver which performs at 10 GHz. High-Q passives and three-dimensional interconnects allow for the design oh high-cost, high density circuits that also exhibit very high performance.

VI. ACKNOWLEDGEMENTS

The work was performed under the DARPA TEAM Project

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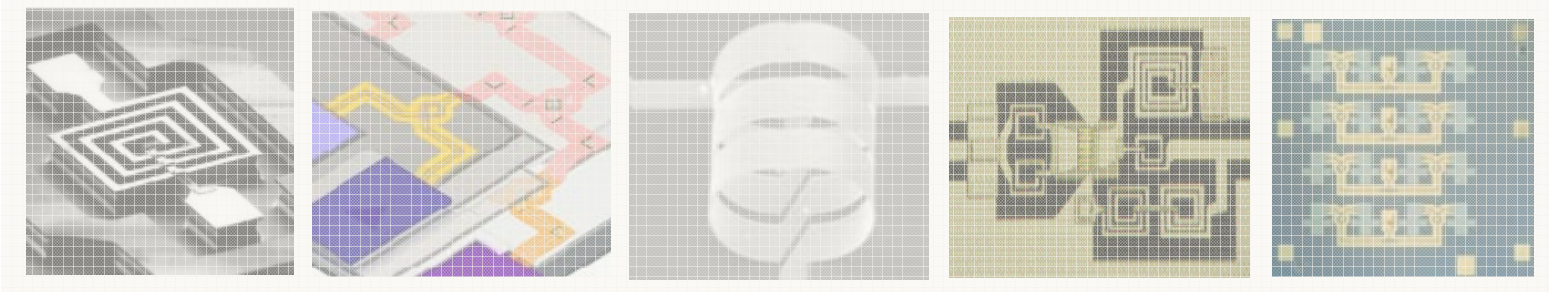


College of Engineering

Heterogeneous On-Wafer and Multilayer Integration

Linda Katehi, Saeed Mohammadi and William Chappell* (Speaker)

Purdue University, West Lafayette

Michael Steer, Angus Kingon

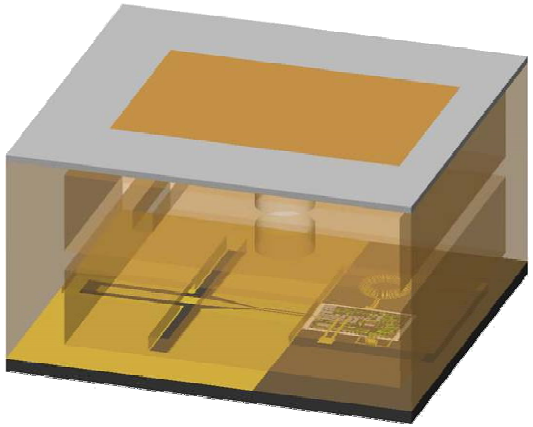
North Carolina State University, Rayleigh, North Carolina

Barry Perlman

CERDEC, US Army RDECOM, Fort Monmouth, N. J.

NC STATE UNIVERSITY

Outline

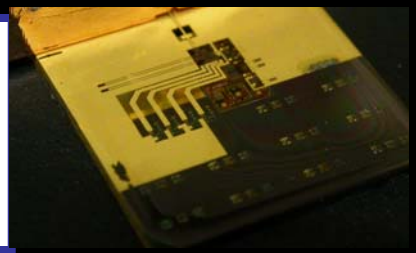


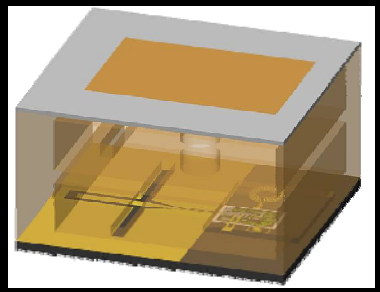
- *Heterogeneous Integration of IC's*
  - *Silicon in Silicon RFIC Wafer Integration*
  - *High-Q Wafer Scale Passive Components*
- *High-Q Filter Integration – RF Cube*
  - *Multilayer High Quality Filters (Q's > 1,000)*
  - *Tunable Filters (1.5:1 Tuning ratios with Q's > 800)*
- *Demonstration of Wafer Scale Integrated RFIC*
  - *10 GHz and 24 GHz Receiver Examples*
- *Integrated On-Wafer Antennas and Future Large Array Systems*

Problem Statement

- ***Problem: The push towards integration onto IC (mixed signal or RFIC integration) is often incompatible with military needs.***
  - ***Large Non-recurring Engineering Costs***
  - ***Design at Central Locations***
  - ***Non-optimal Material Choices (Sub-optimal Performance)***
- ***Solution: Massively Integrated Hybrid Systems***
  - ***Flexibility of Hybrid with Large Scale Integration of SOC***
  - ***Integration at the Wafer Scale Using Silicon Interposer***

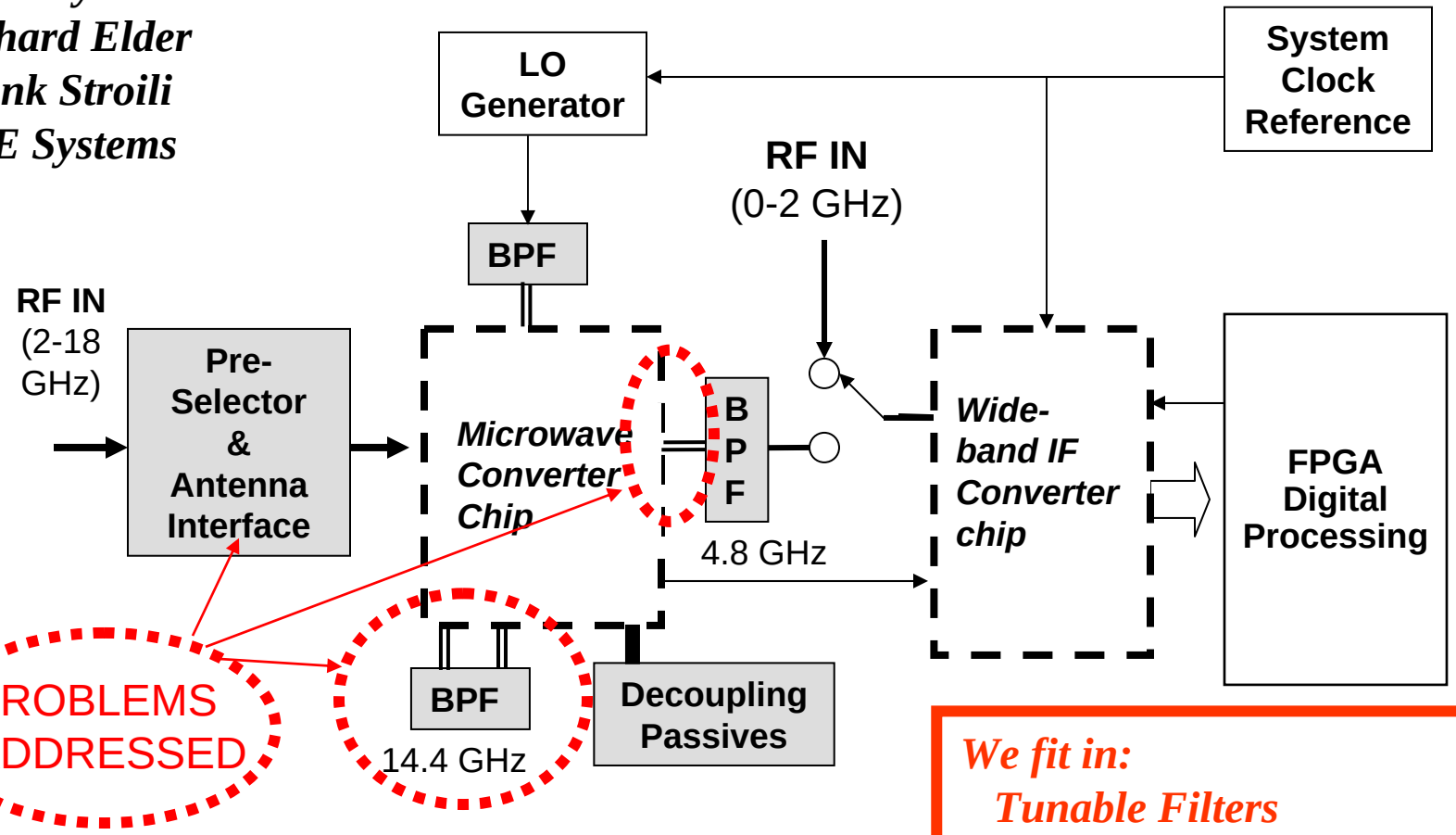
Wafer-in-Wafer and 3-D Heterogeneous Integration





Typical EW System

Courtesy:
Richard Elder
Frank Stroili
BAE Systems



‖ = *Differential Signal Path*

▭ = *Target insertions*

We fit in:
Tunable Filters
Differential Signal Paths
Embedded Passives

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Heterogeneous Integration Concept

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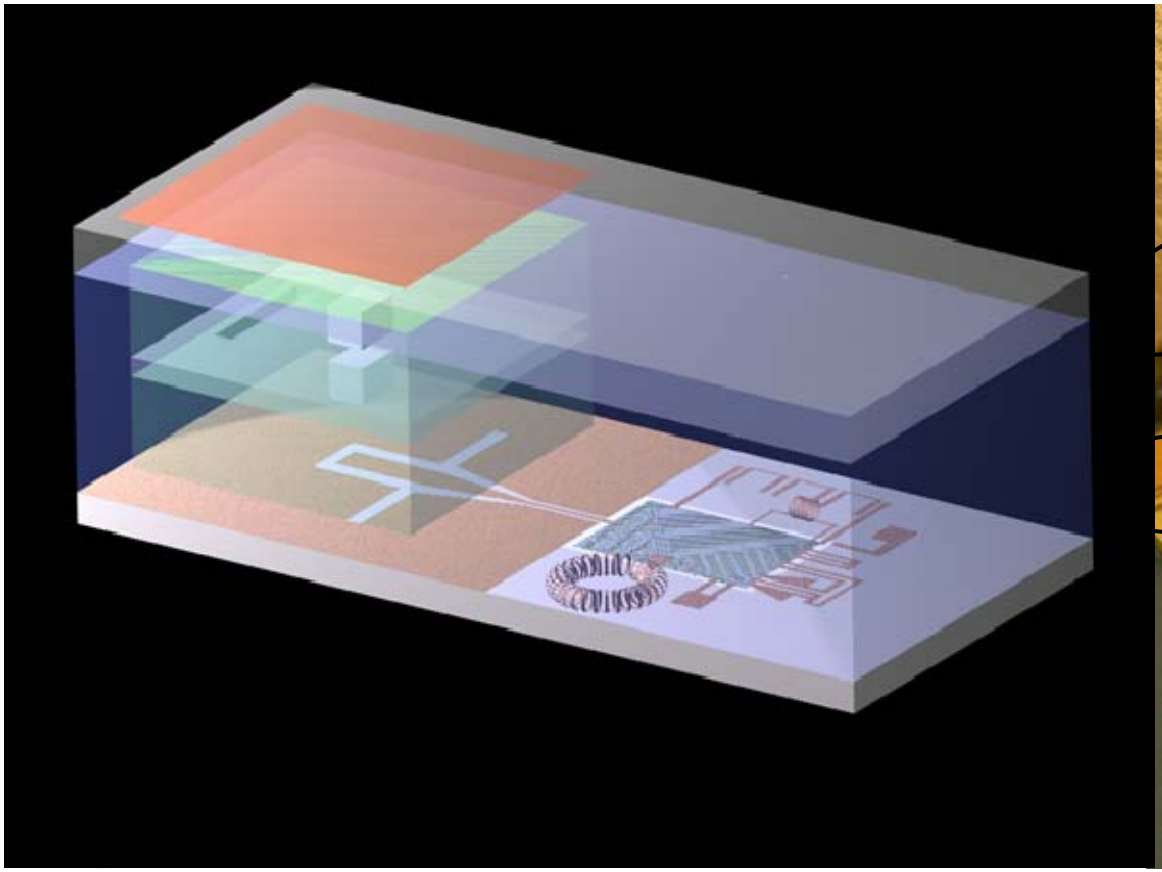
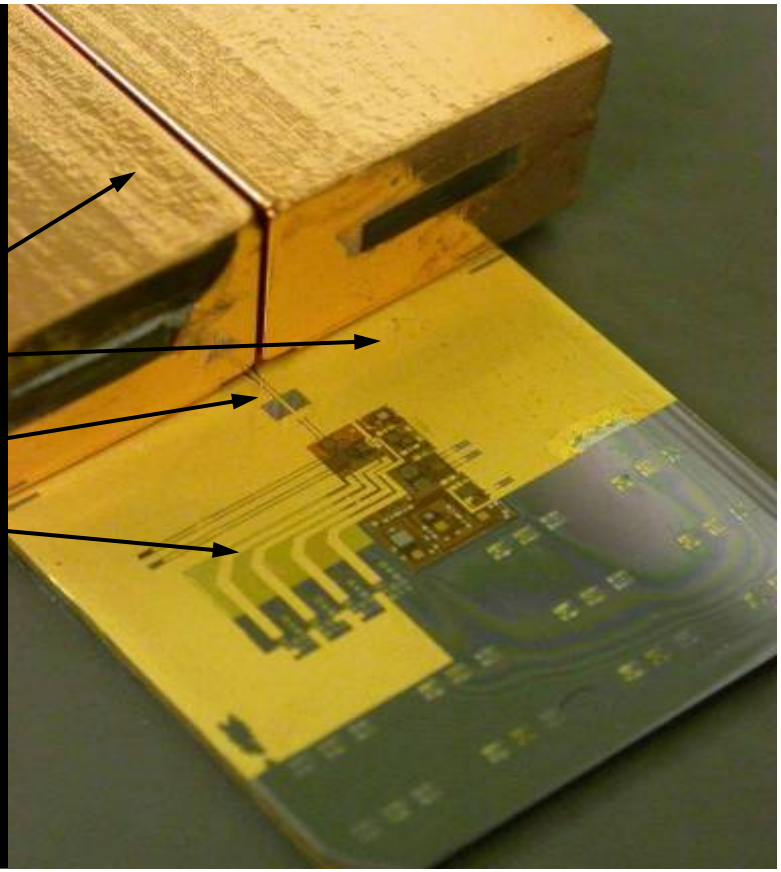
Utilize Wafer Scale Silicon in Silicon Integration and Multilayer Packaging to Create Miniature Self-Contained RF and Microwave Systems





Fully Integrated Chip/Si-Interposer

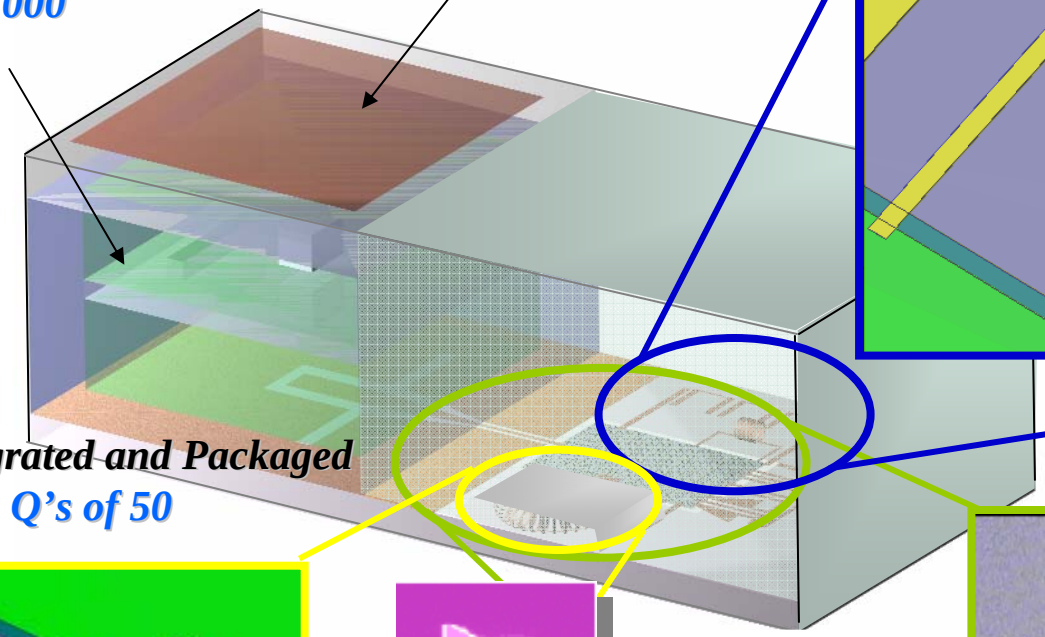
Distributed Elements Integrated and Packaged in Interposer: Q's over 100

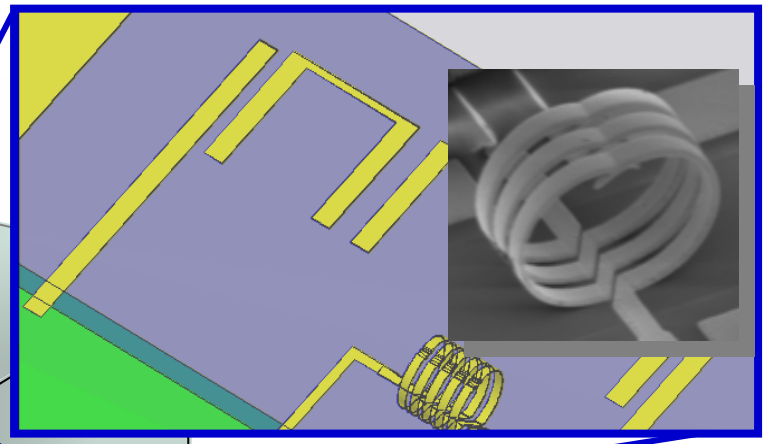
Antenna

Eff> 80%

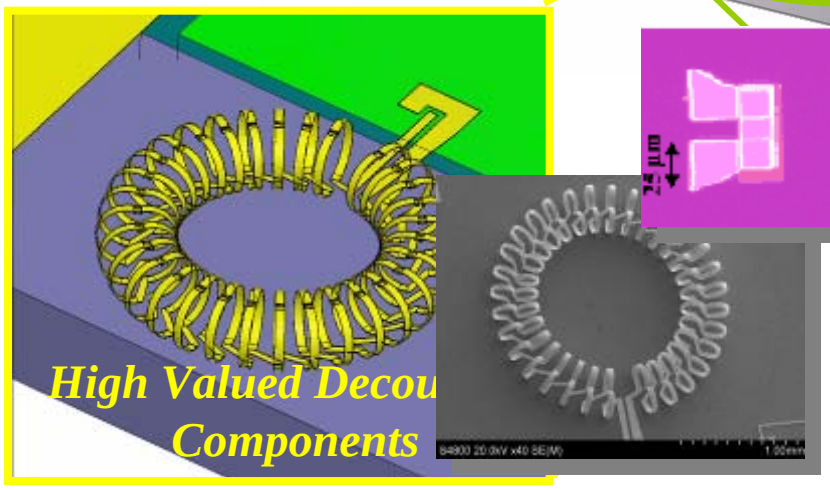
Integrated High-Q Cavity

Q>1000

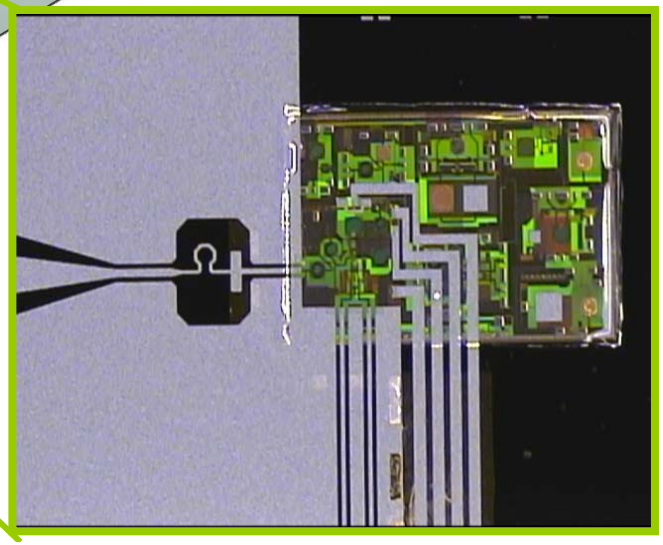




Lumped Integrated and Packaged in Interposer: Q's of 50



RFIC: Q's of 10



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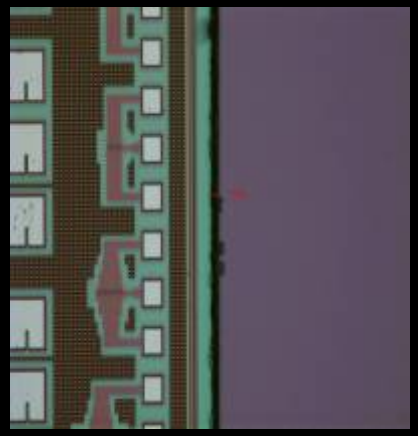
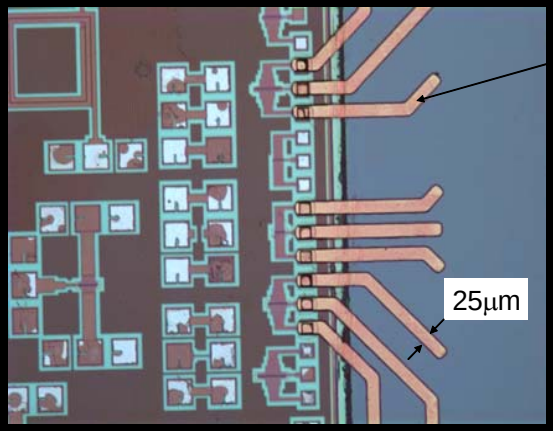
Heterogeneous Integration at the Chip Level

DARPA

24GHz fully integrated receiver



IC Interposer

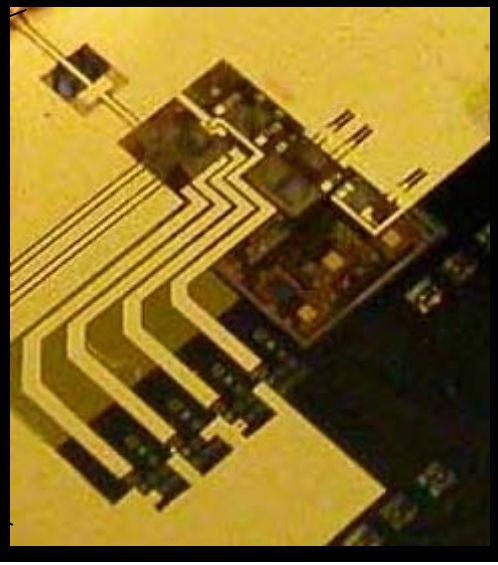


Post metallized for I/O's

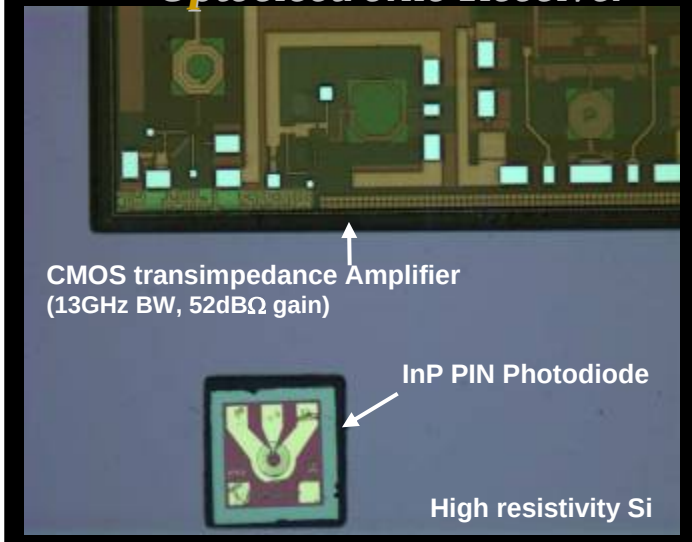
5 to 25 micron interconnect width was easily achieved

(SAWLIT) Wafer Level Integration

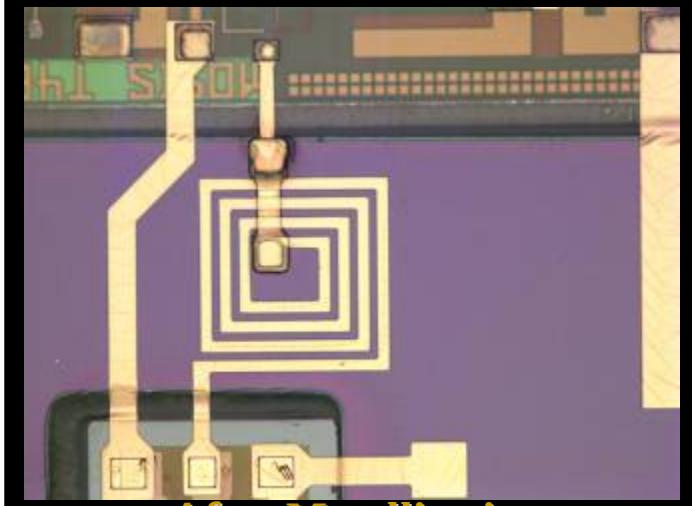
View of Assembled IC in Interposer



15Gb/sec CMOS/InP Optoelectronic Receiver



Before Metallization



After Metallization

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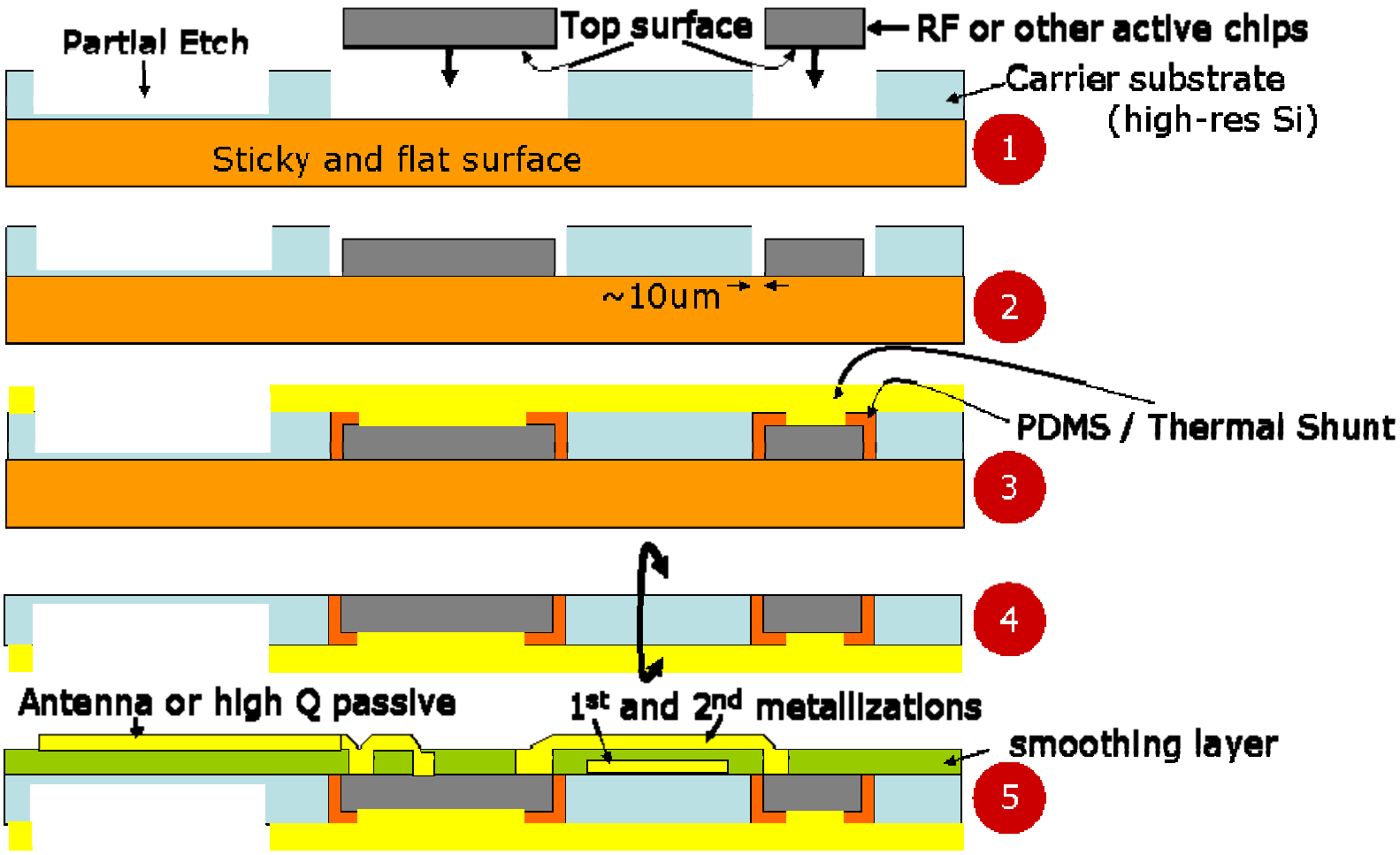
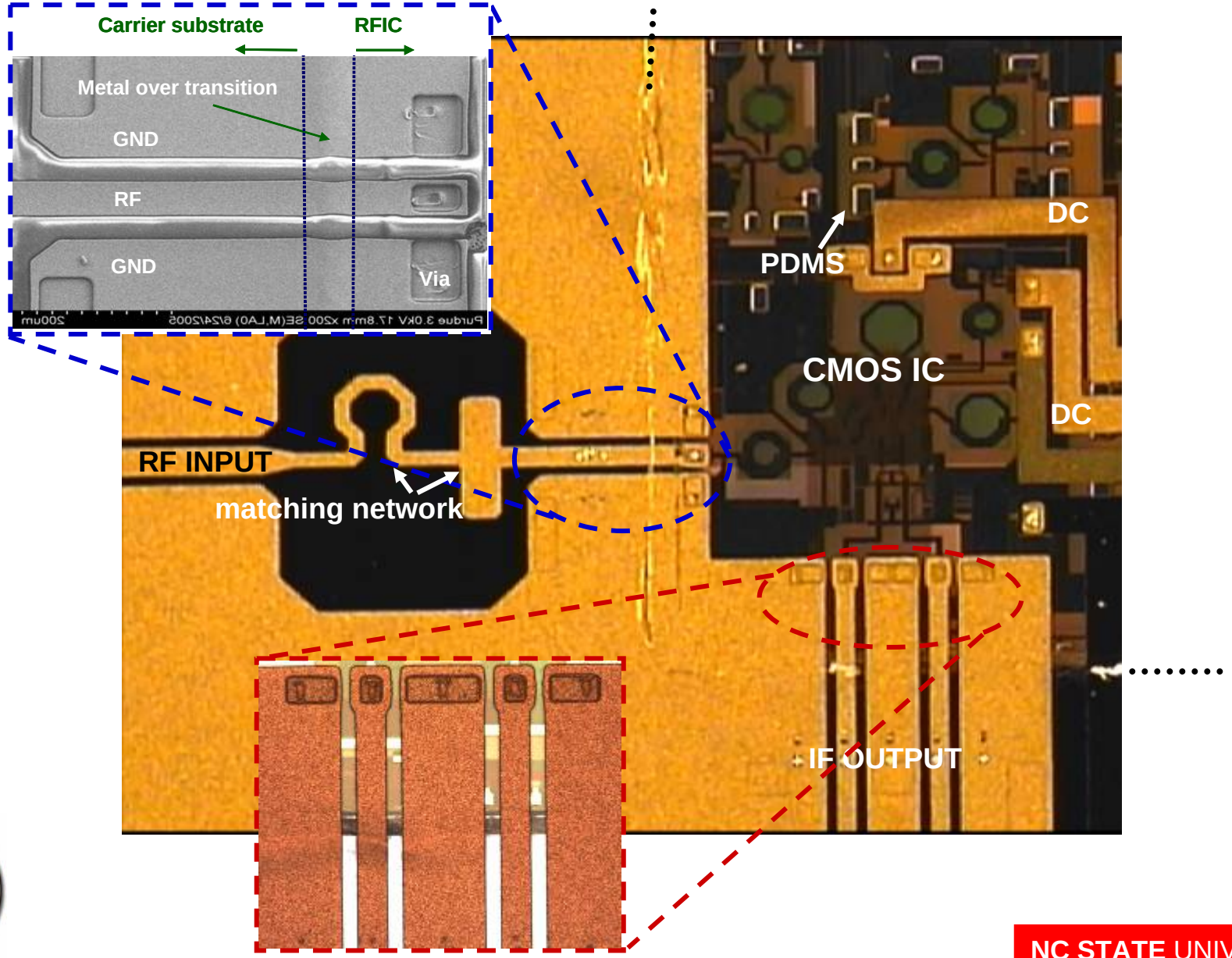
SAWLIT Fabrication

Self Aligned Wafer Level Integration Technology

DARPA



SAWLIT for 10GHz Receiver



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Advantages Specific to Military Systems

Heterogeneous integration (Massively Integrated Hybrid Circuits)

- Designs at Numerous Locations with Optimal Materials as Needed.

Lower power dissipation :

- Seamless integration between IC's with no line drivers or parasitic pad reactance

Utilize different technologies / optimize cost and performance :

- Example: use 0.13um SiGe/CMOS for RF receiver, GaAs for RF PA, RF MEMS for transmit receive switch, High-ρ interposer for passives and 0.25um CMOS for IF amplifier / control circuits.

Implement passives on carrier substrate (interposer):

- Smaller size active chips on a Low Loss Substrate

Mask programmable:

- Same actives for RF but different routing and different passives to create different circuits.

Off Chip Wafer Level Components
High-Q 3D Inductors

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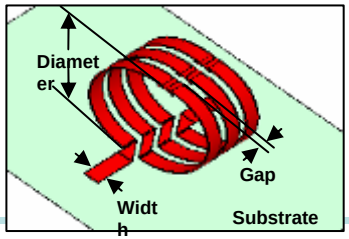
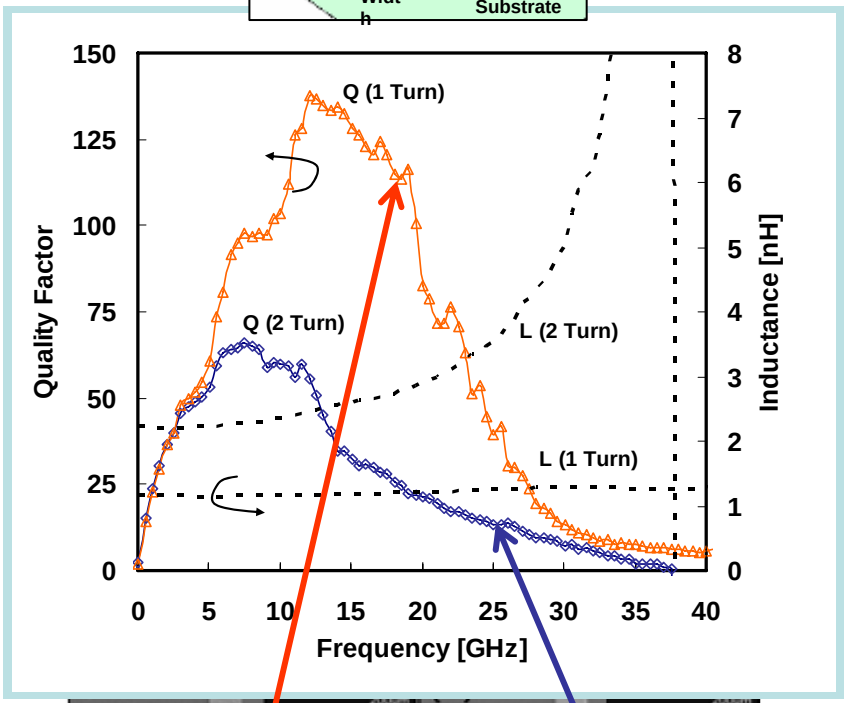
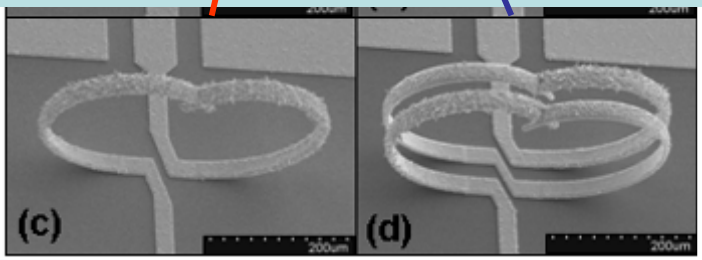
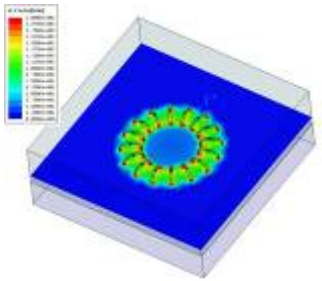
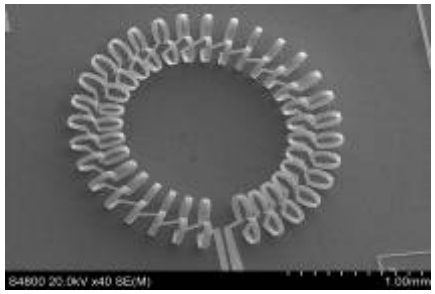
3D inductors based on Au/Cr stressed metal combination

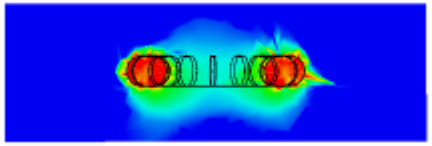












FOM=(Inductance-nH) x (Quality factor)

- *One-Turn Micromachined Inductors: FOM=150*
- *Toroidal: FOM=361*

Substrate	# of turn	L (nH)	Q_{max}
Low-Resistivity (10 -20Ω·cm)	*16*	***13.8***	***4.98***
	31	***28.2***	***4.11***
High-Resistivity (>10 kΩ·cm)	*16*	***12.9***	***18.5***
	31	***25.4***	***14.2***

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Off Chip Wafer Level Components
3D Transformers

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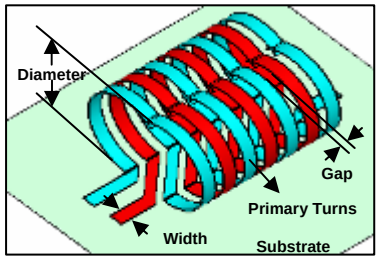
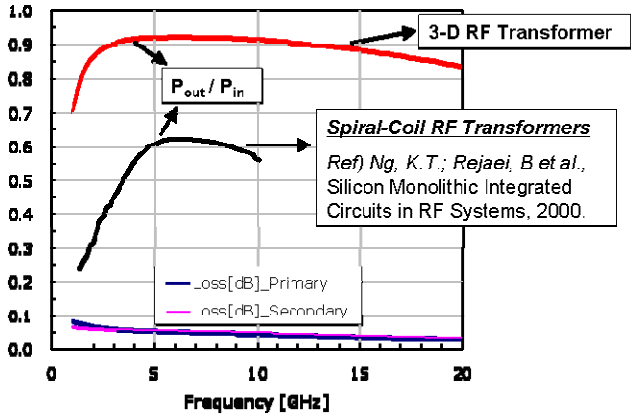
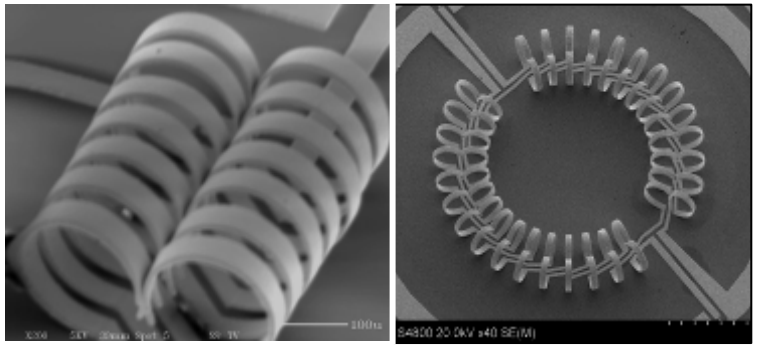
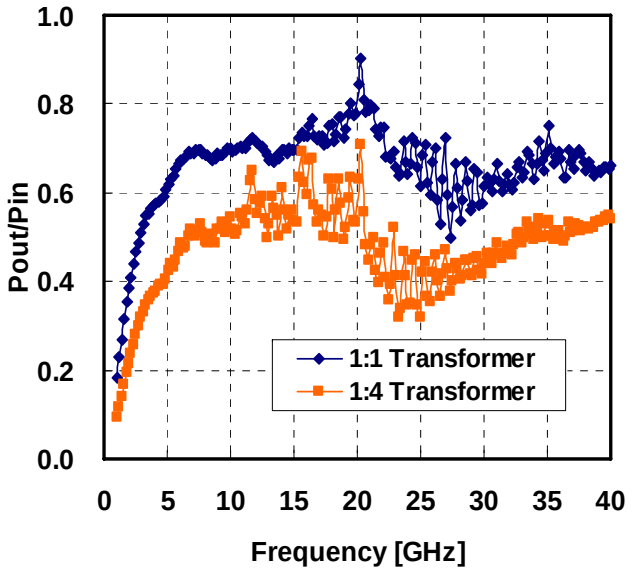
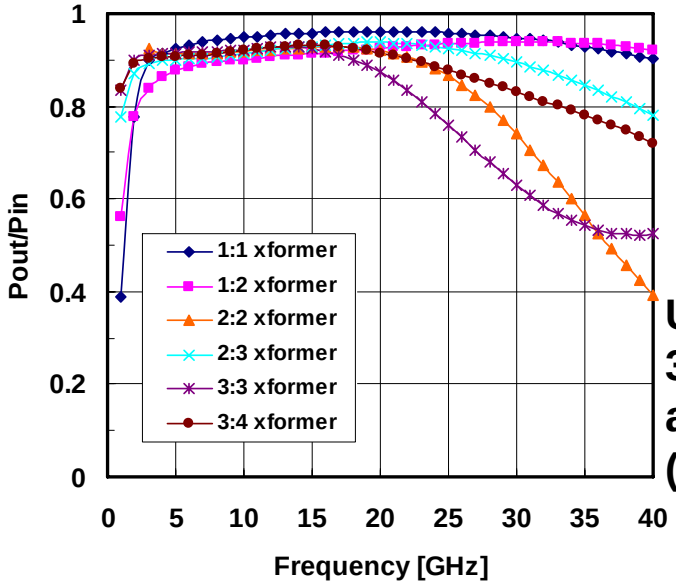
3:4 3D Transformers (95% power efficiency)











Unlike spiral transformers 3D transformers are extremely wideband (3GHz<BW<~35GHz)

*U.S. Patent Filed

CECOM

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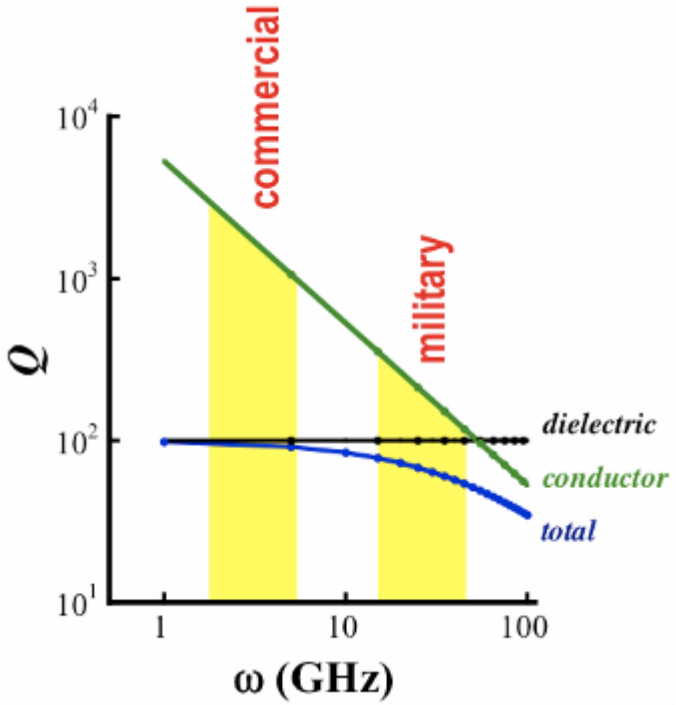
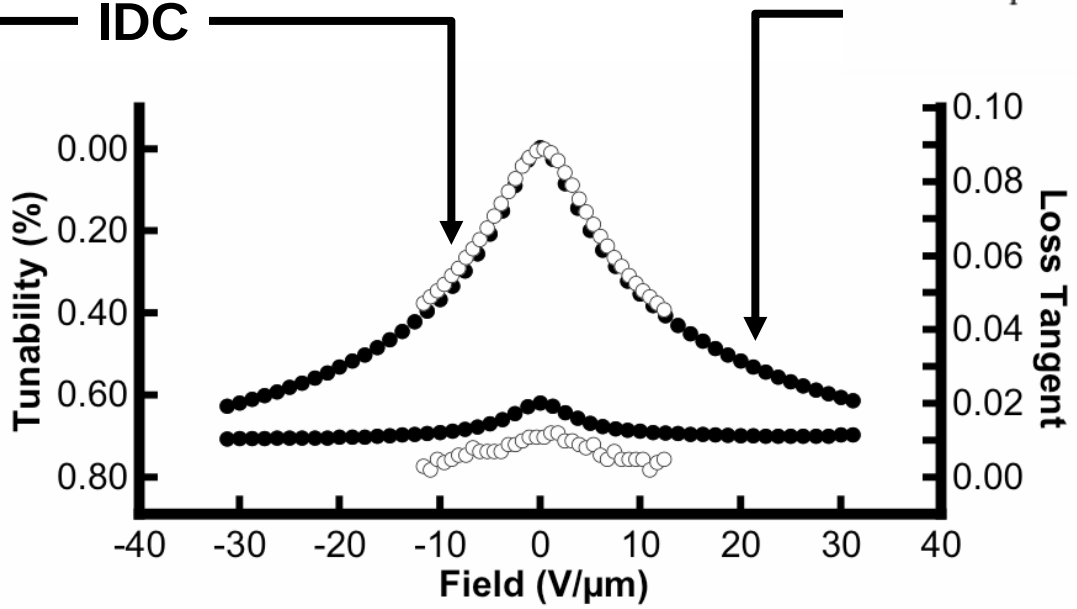
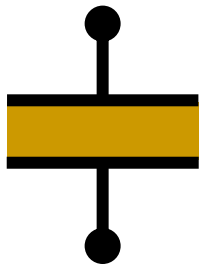
BST Components

- *Embedded Passive, Agility using BST varactors*
  - *Explore New Architecture*
  - *Tunable Filters; Matching Networks; VCOs*
  - *Embedded High-Valued Passives*



BST Varactors





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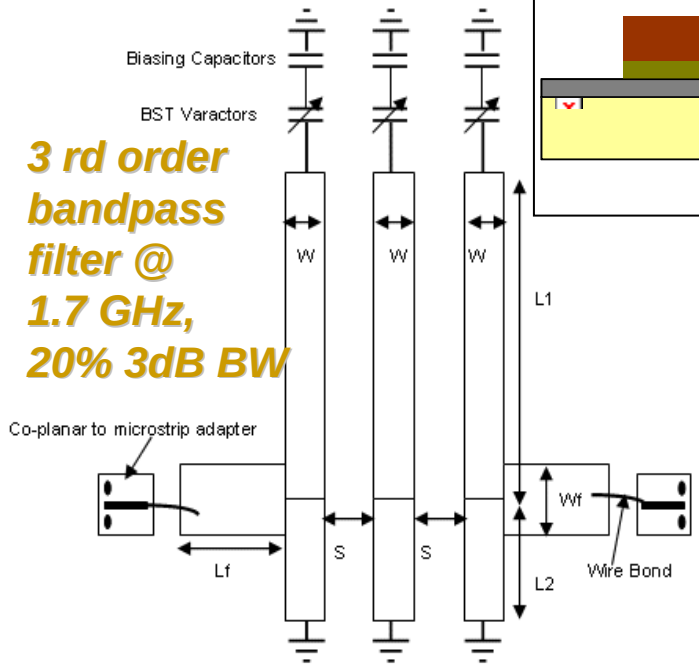
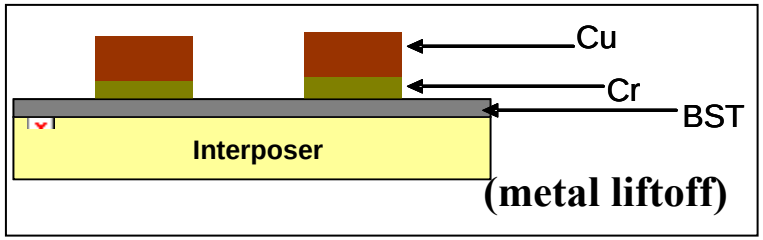
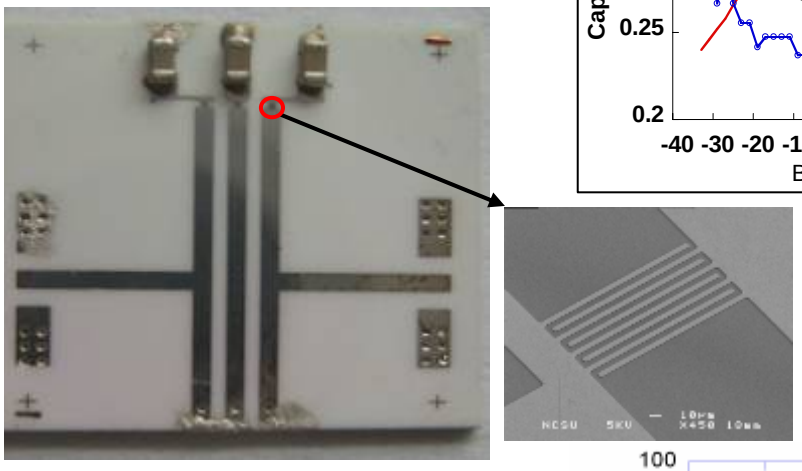
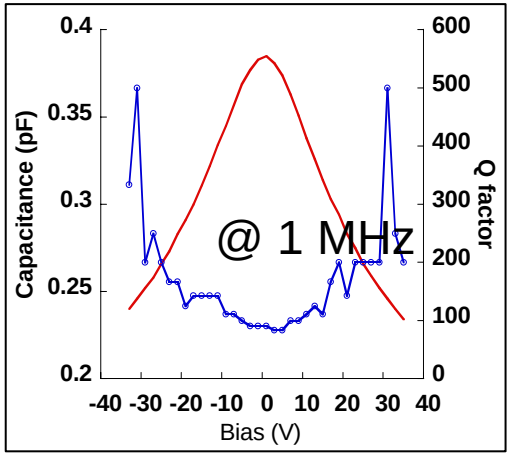
Tunable Lumped Element Bandpass Filters



3 rd order bandpass filter @ 1.7 GHz, 20% 3dB BW

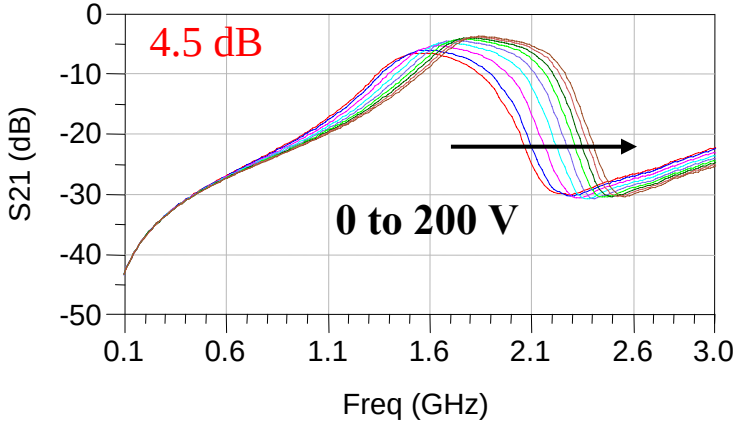




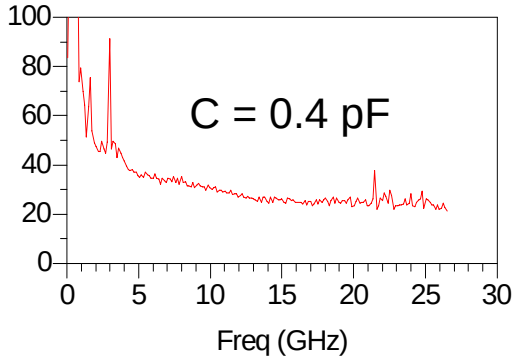


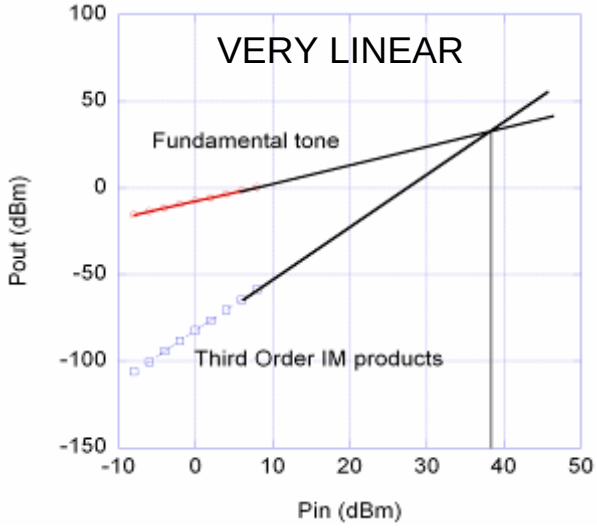
50% varactor tuning leads to 25% tuning of the filter

(REDUCE TO 2.5 dB in 12 months)



Q factor of 28 @ 26 GHz



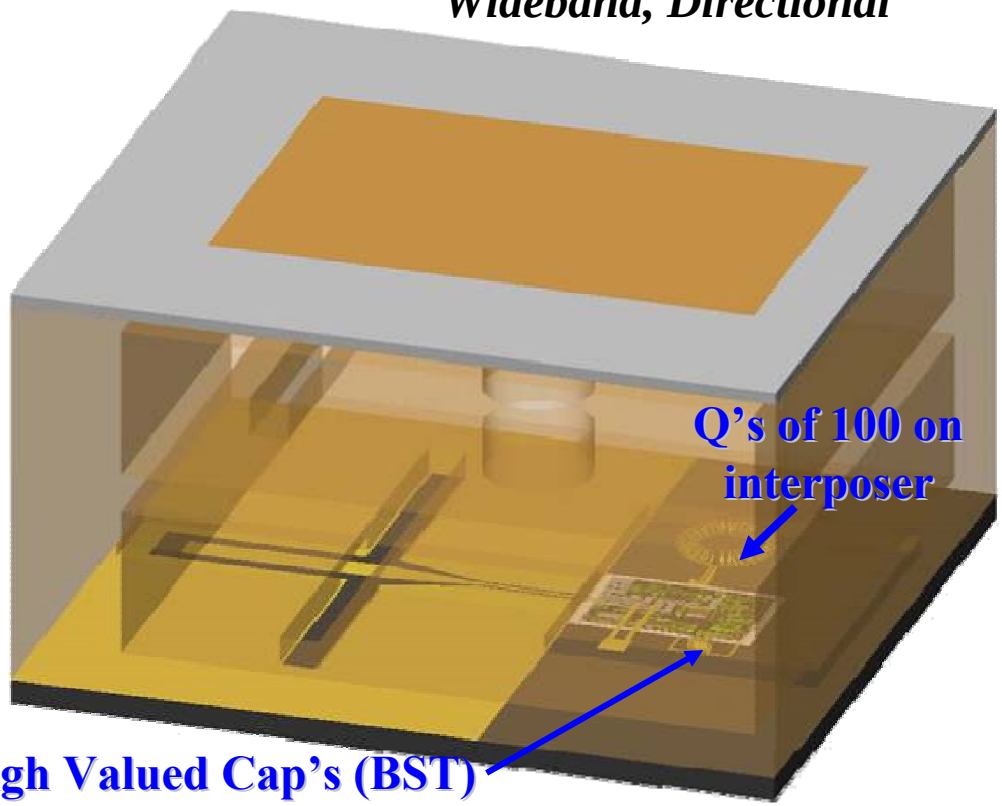


Heterogeneous RF Cube

Filter/ Antenna Integration : Tight integration of high quality components (Q>1000) with an IBM7RF RFIC in a silicon carrier wafer and highly efficient antennas

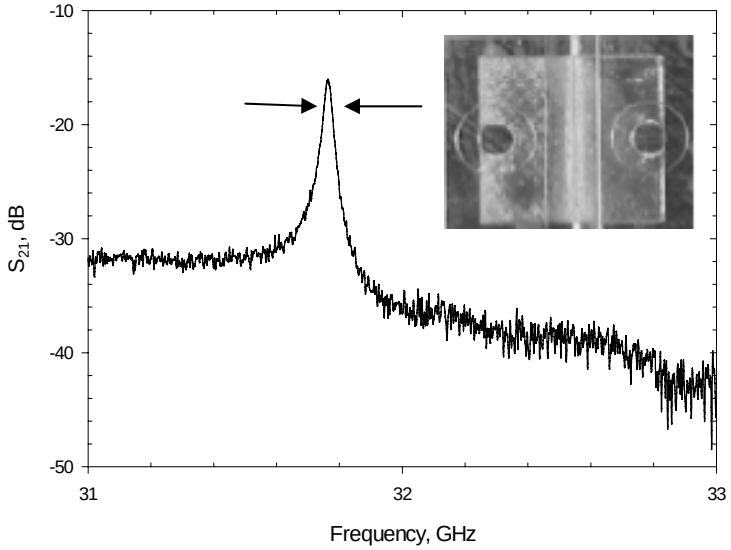
- *Layer by Layer Packages to Create Three-Dimensional Integrated Components*
- *Q> 1,000 - Enables low loss filtering*
- *Protection of Circuitry Without Degradation*
- *Eliminate Deficiencies of On-Chip Antennas*

Efficiency > 70%, Wideband, Directional



Q's of 1000 in multilayer filter (preselect filtering)

Cavity Based Integrated Filters



Single Embedded Cavity Resonator:

200 Layers of Polymer:
Demonstrated Unloaded Q's of 3,000

Figure of Merit= Q/Area = $6{,}000/\lambda^2$

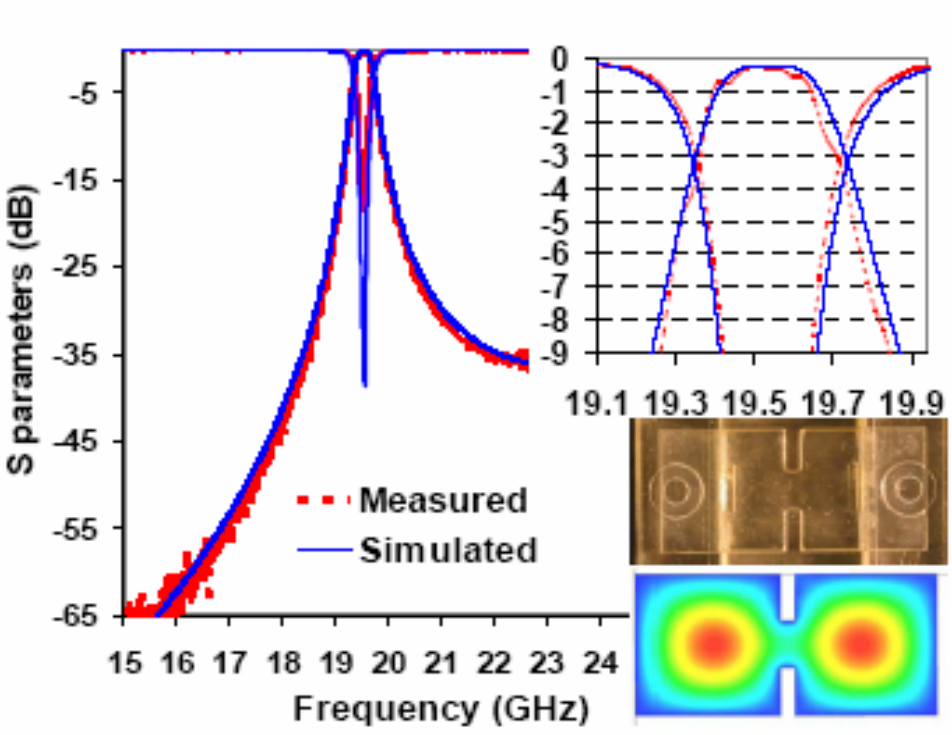
Horizontal Integrated Cavities

200 Layers of Polymer:

Insertion loss = 0.262 dB

BW = 1.83% - Q~ 3,000

FOM= Q/Area = $6000/\lambda^2$

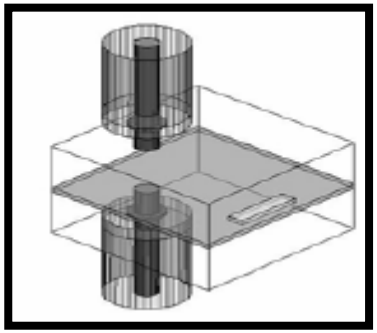


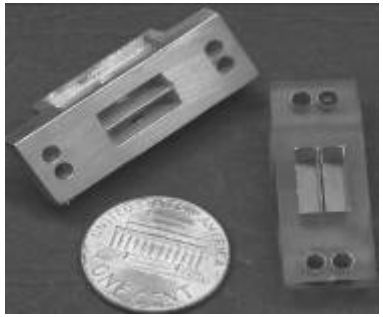
High-Q Reduced Size Filters

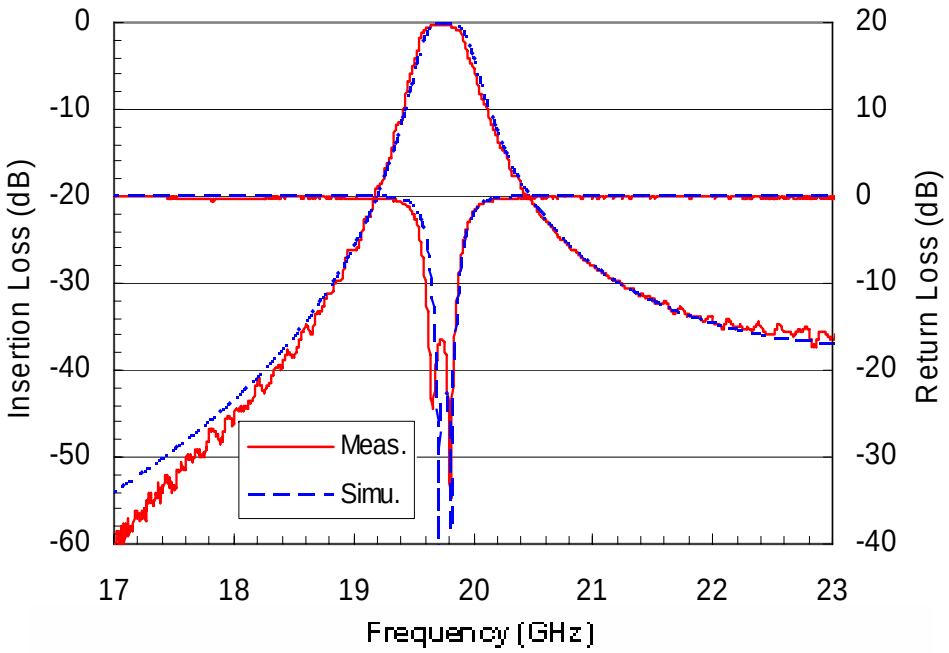
Reduced Size Vertically Integrated Cavities

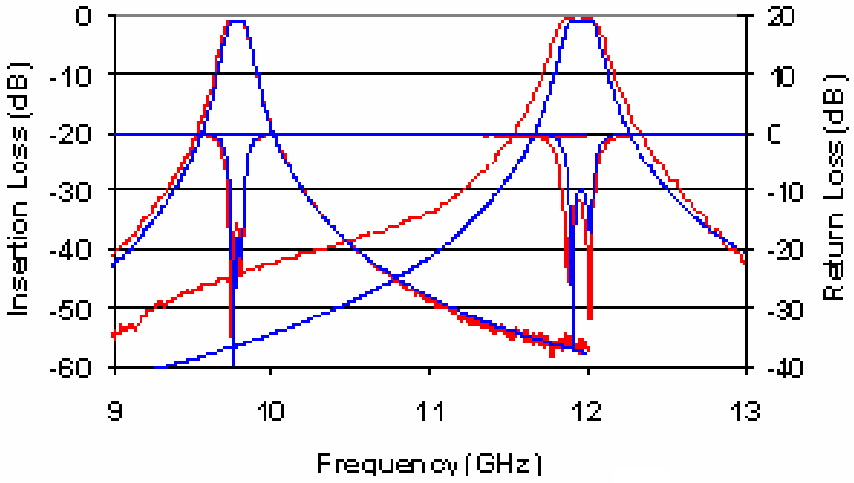
I.L. = 0.262 dB, BW = 1.83 %

Q~ 3,000, FOM = 12,346/λ^2





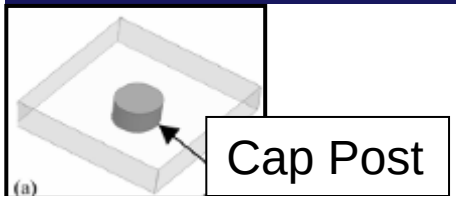


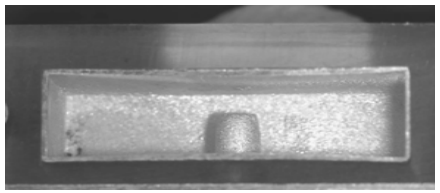


Evanescent Filter: Reduction to ¼ of Cavity

I.L. = 0.35 dB, BW = 1.8 %

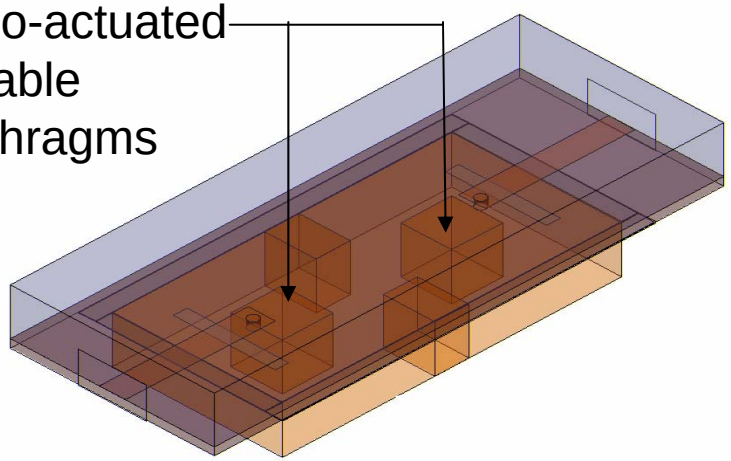
Q's ~ 1200, FOM = 5,164/λ^2

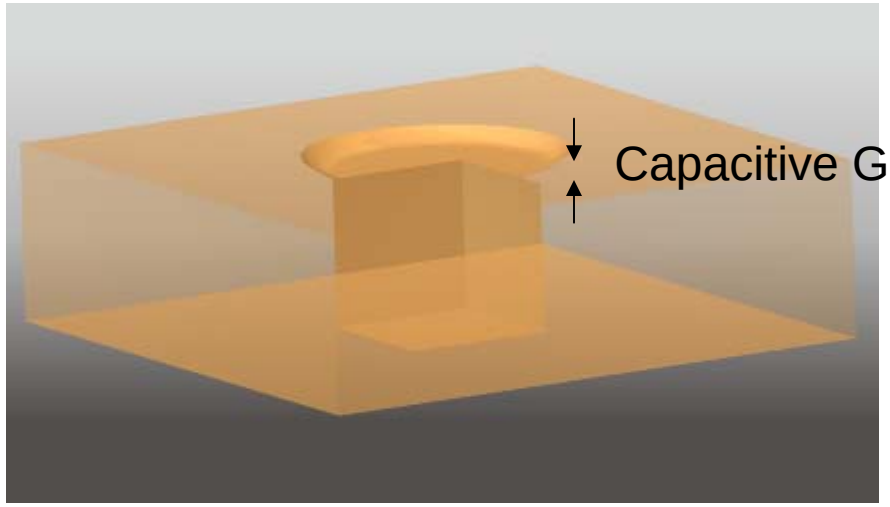


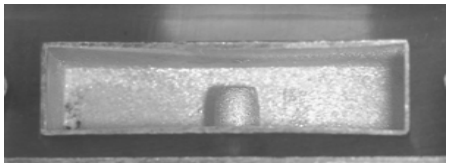


Tunable High-Q Filters

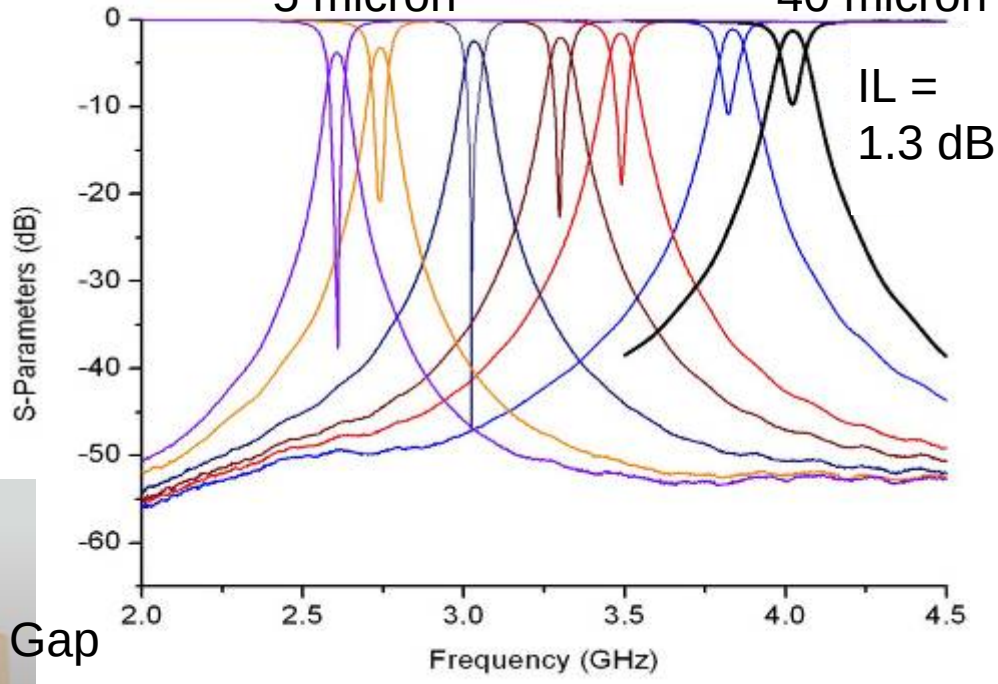
Piezo-actuated Tunable diaphragms







5 micron ← 40 micron



Measured Tuned Evanescent Cavity 2-Pole Filter

Unloaded Q's ~ 900
Insertion Loss < 1.3 dB for a 1.75 % Filter

Preselect Tuning is Now Possible Without Degradation in Performance

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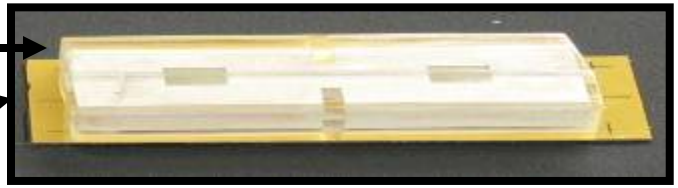
Silicon Interposer Integrated Evanescent Filters

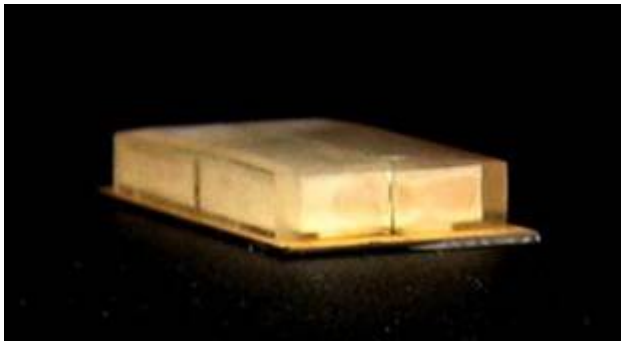
DARPA

10.3 GHz Filter Results: Measurement and Simulation in Good Agreement.

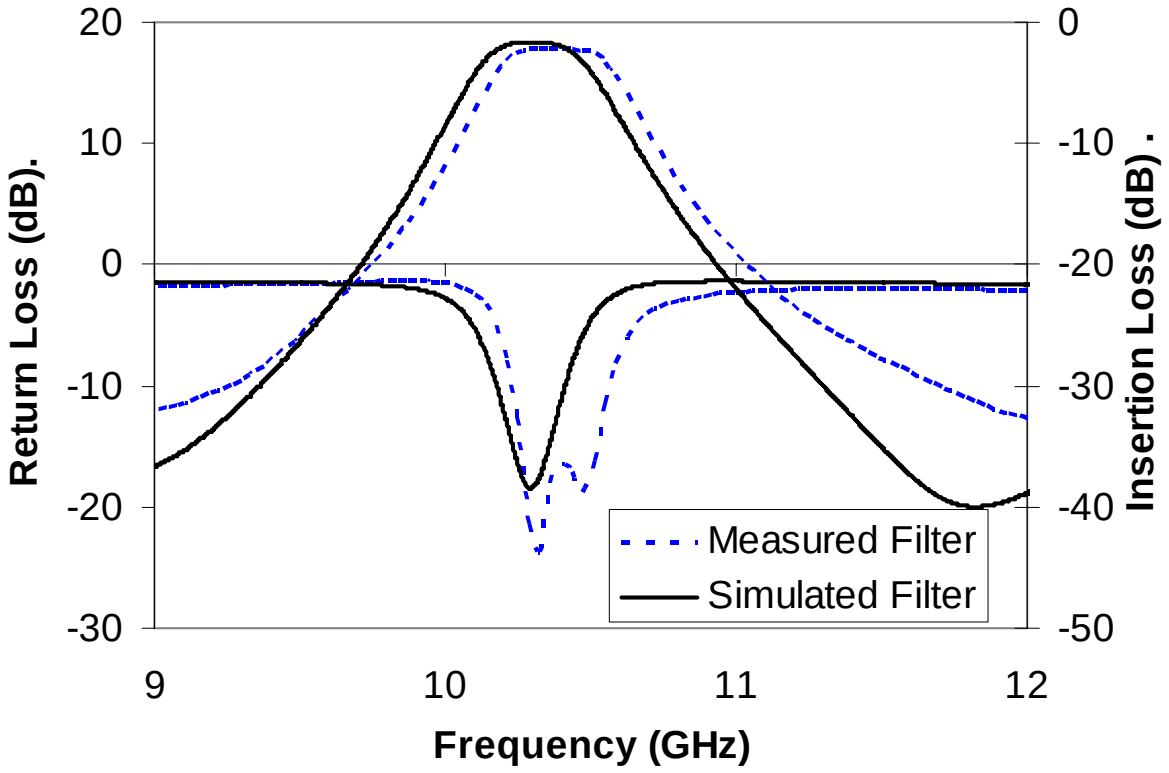
>150 Layers of Laser Cured Polymer

Silicon Interposer





Consistent and Repeatable Results Allows for Integration with RFIC

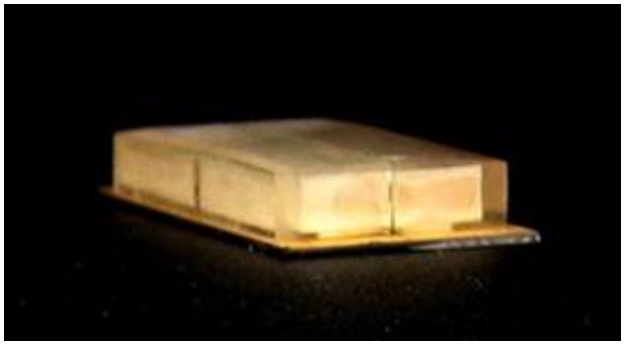


Silicon Interposer Integrated Evanescent Filters

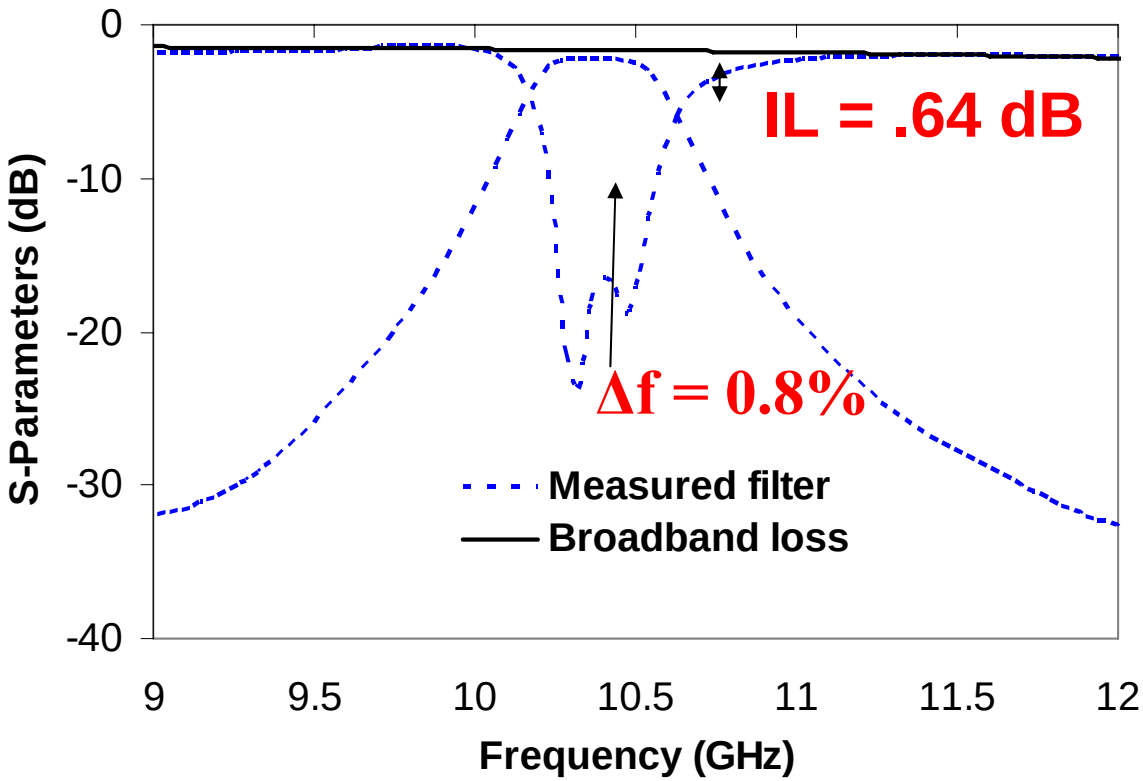
10.3 GHz Filter Results: Meas and Sim in Good Agreement.

IL = -.64 dB for ~ 4 % filter.

Center Fo = 0.8 % off of design frequency



Consistent and Repeatable Results Allows for Integration with RFIC



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High Efficiency Antenna for Silicon Interposer Integration

DARPA

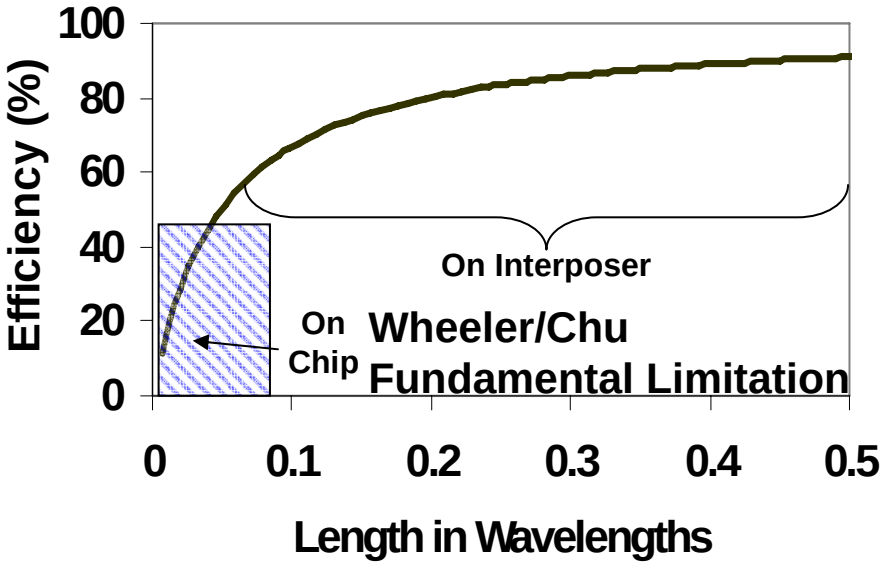
Planar Slot Antenna

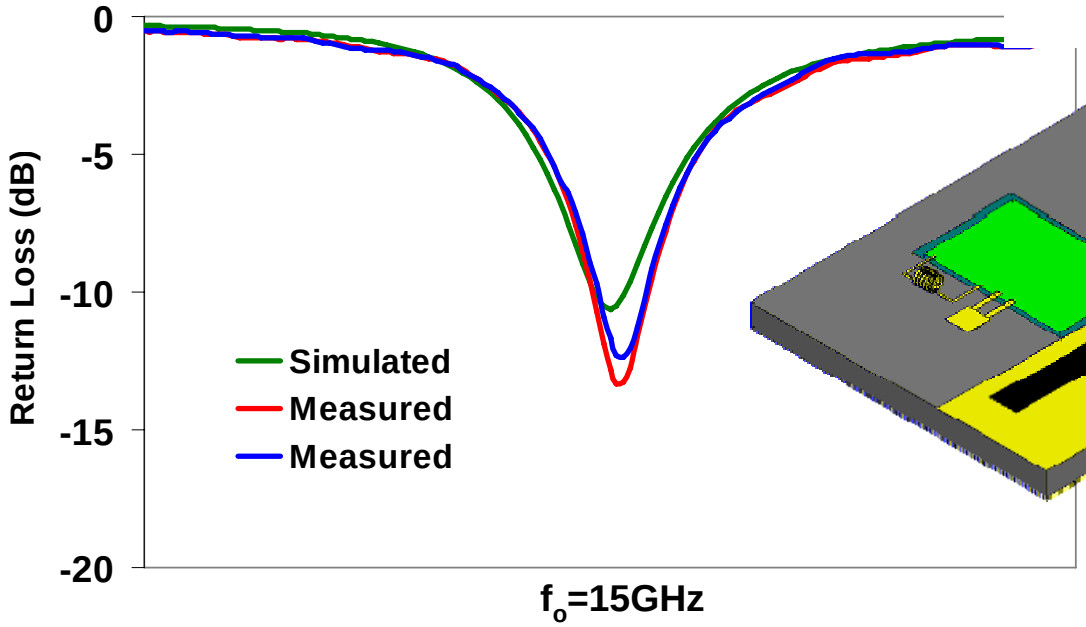
Readily Integrated on Interposer with RFIC/Filter Combination

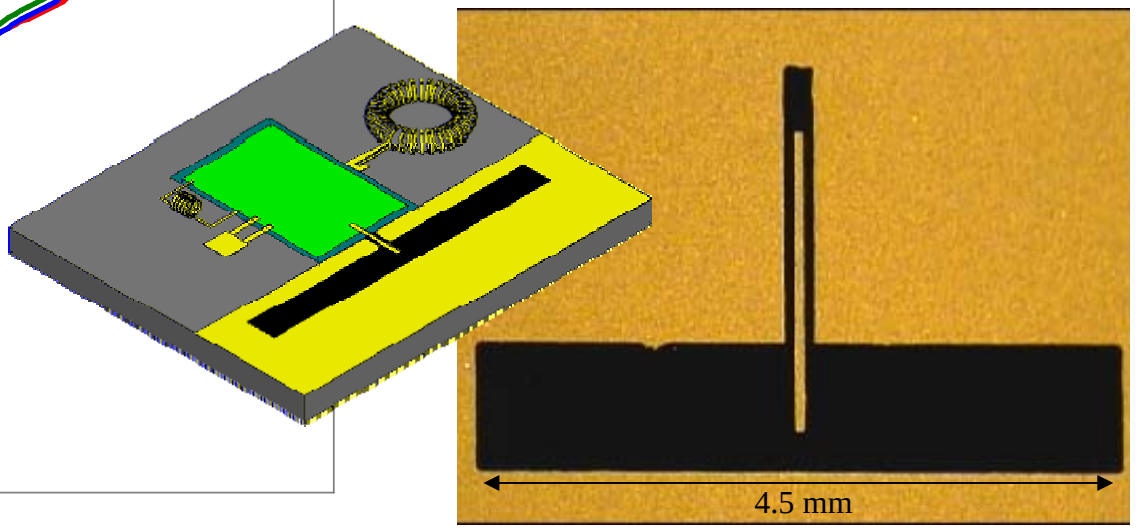
Resonant Frequency - <1% off

Interposer > 85% Efficiency

Improved Bandwidth (3 x $BW_{on\text{-}chip}$)







System Demonstrations
10 GHz Front-End (IBM 7RF CMOS)

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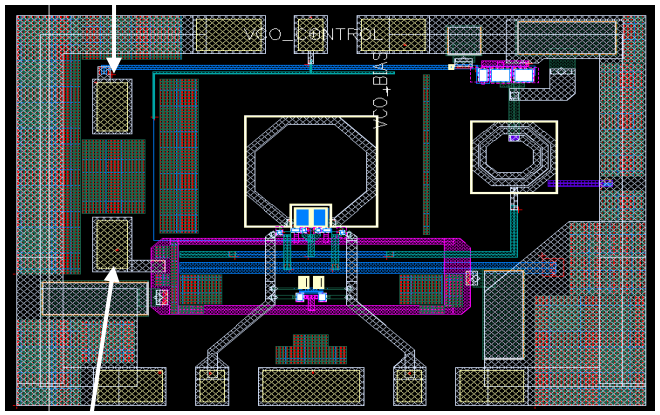
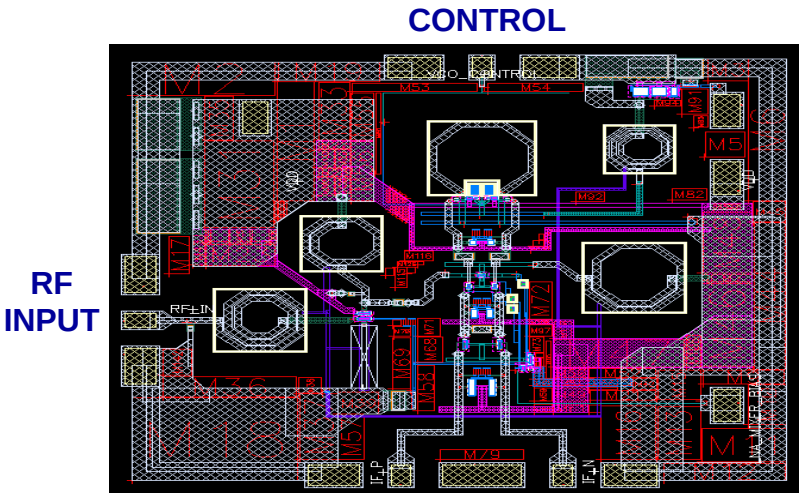
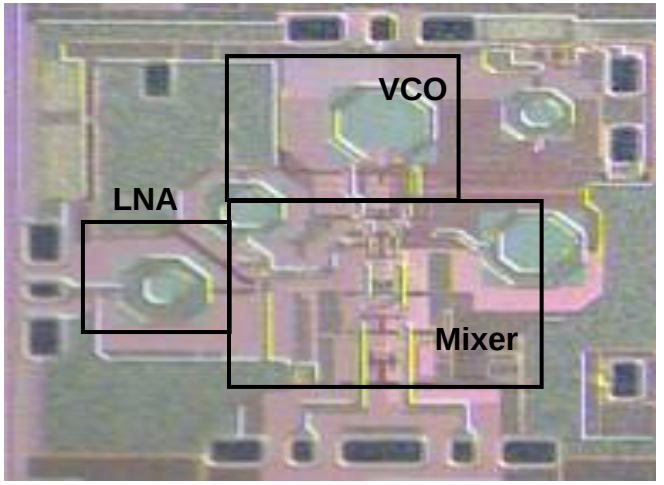
DARPA





VCO (950 μm x 720 μm)



Front-end (LNA + Mixer + VCO)
(1250 μm x 1200 μm)

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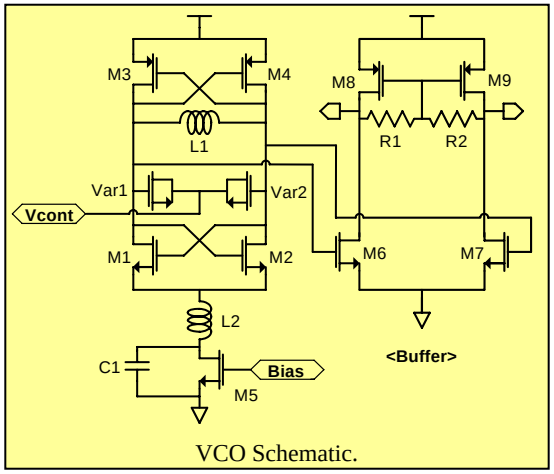
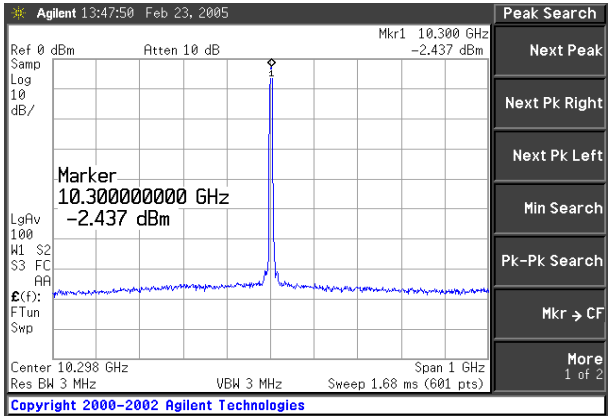
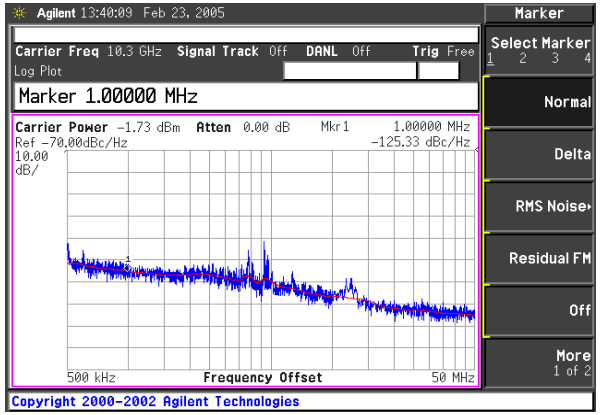
Highly Stable 10GHz CMOS LC Oscillator



VCO Schematic.



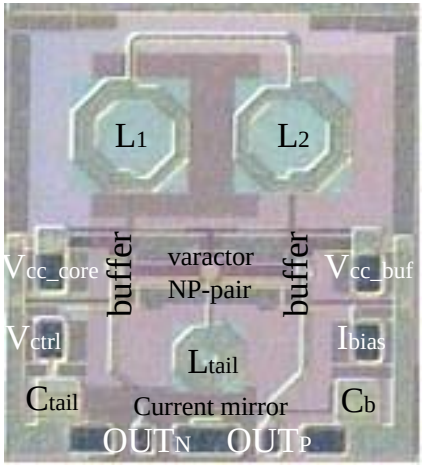
Output spectrum of the VCO @10.3GHz.

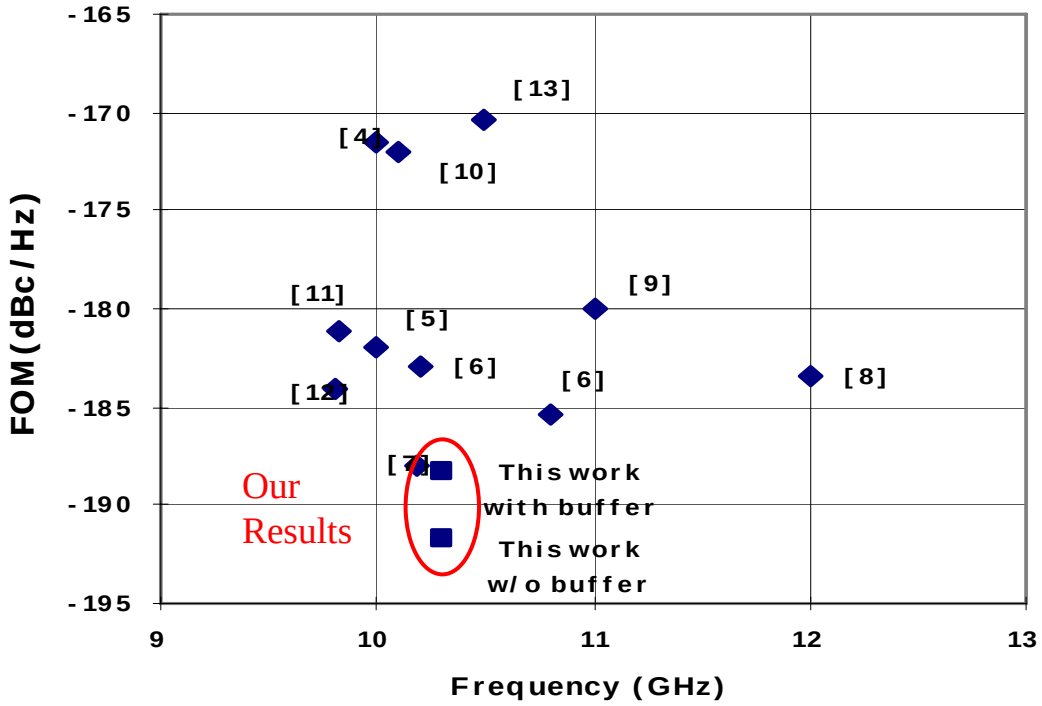


Phase Noise of the the VCO at carrier frequency of 10.3GHz.

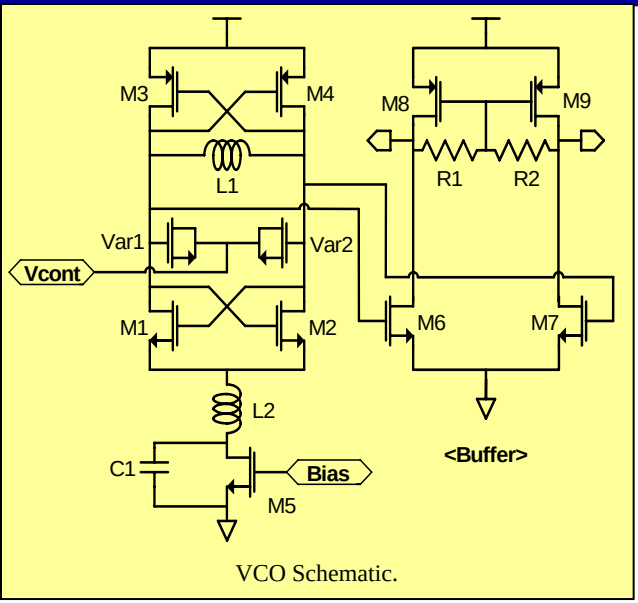
Figure of Merit for VCO (FOM)

$$FOM = PN(f_{offset}) - 20\log\left(\frac{f_o}{f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right)$$

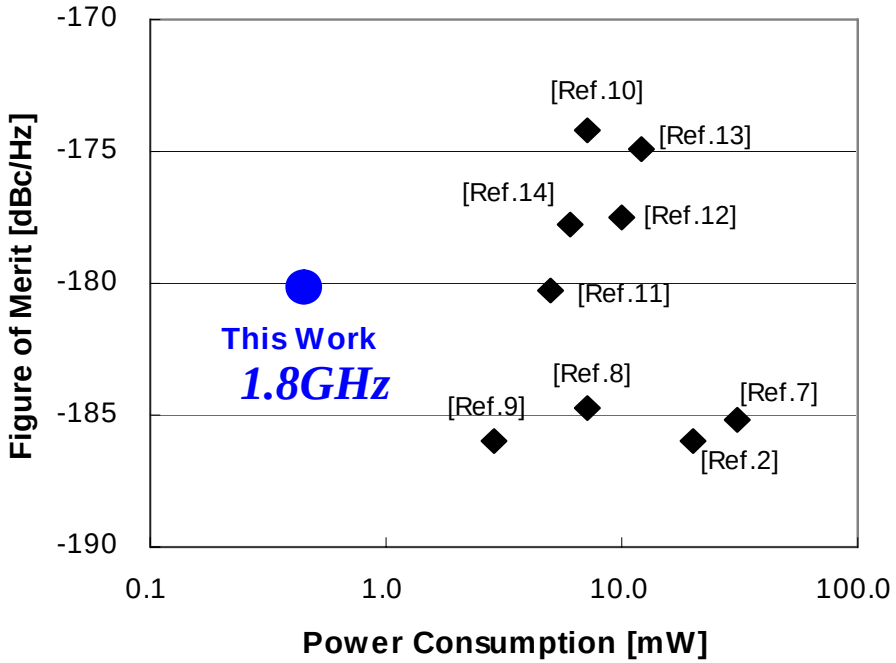




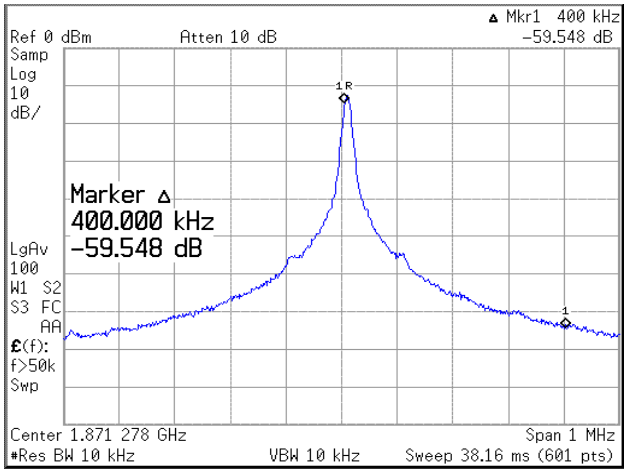
Low Power CMOS LC Oscillator

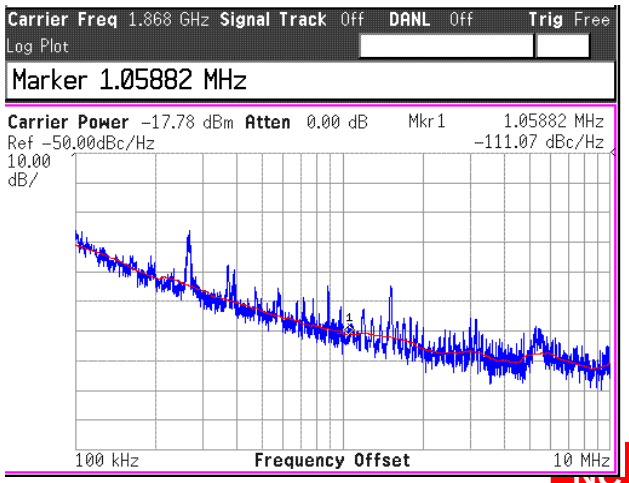


VCO Schematic.



IBM 7RF CMOS





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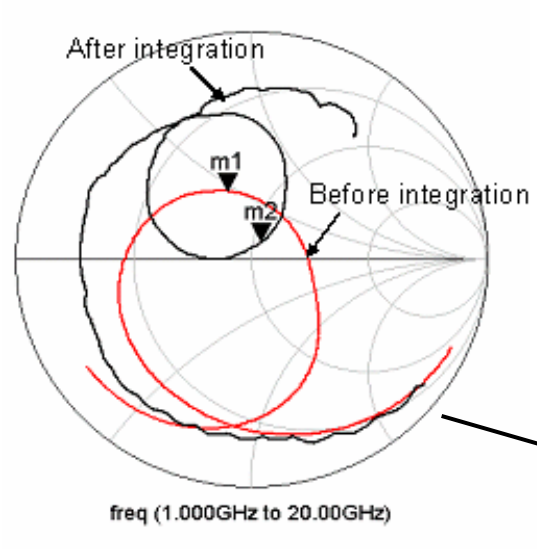
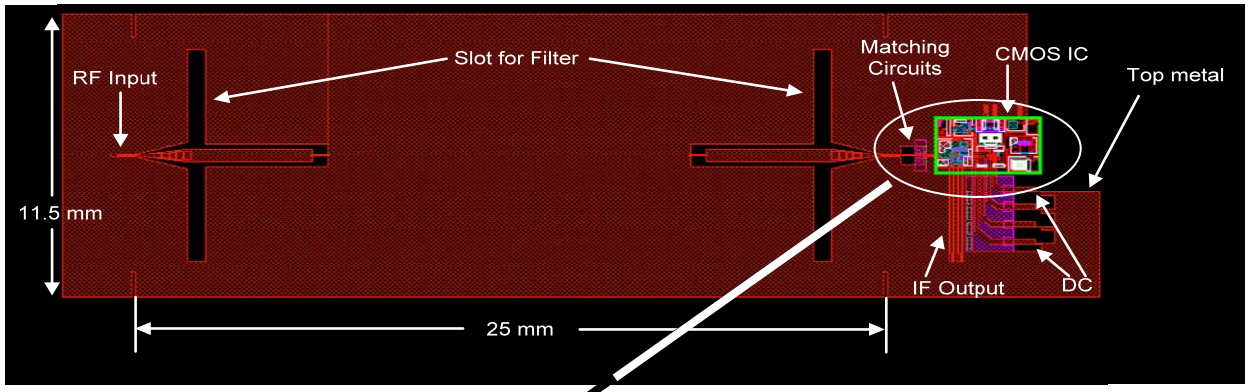
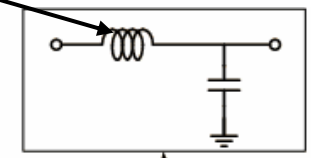
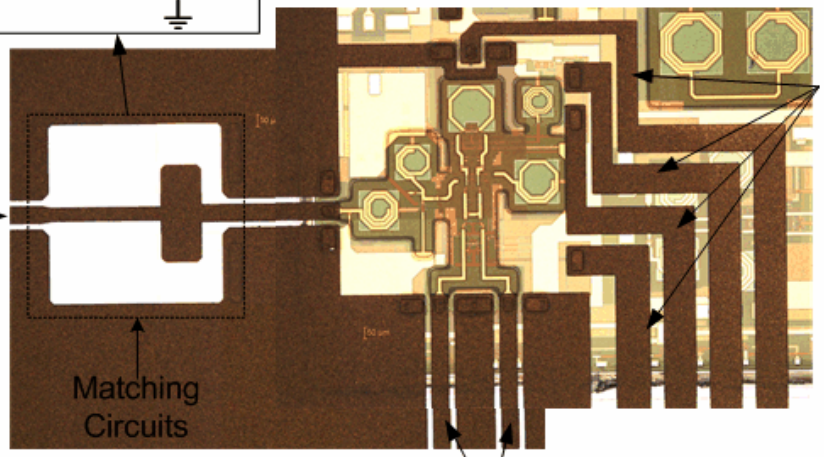
Layout and Photograph of 10GHz Package

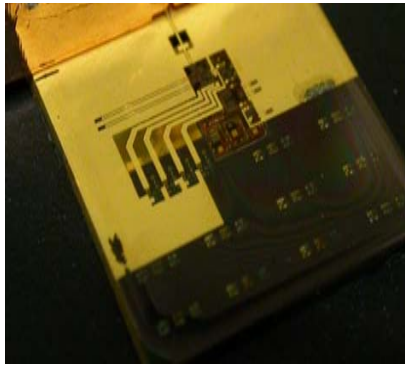




Input matching is improved by embedded matching circuits







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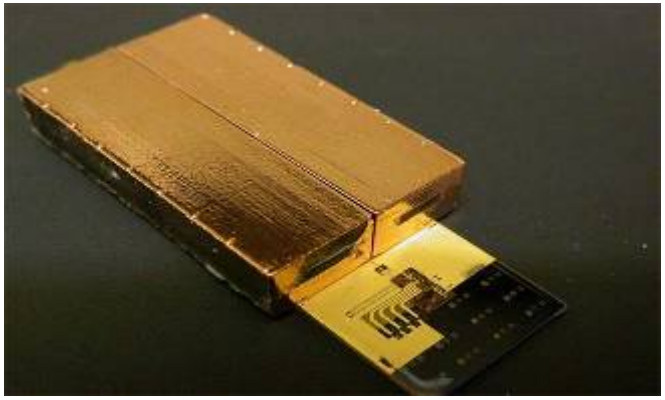
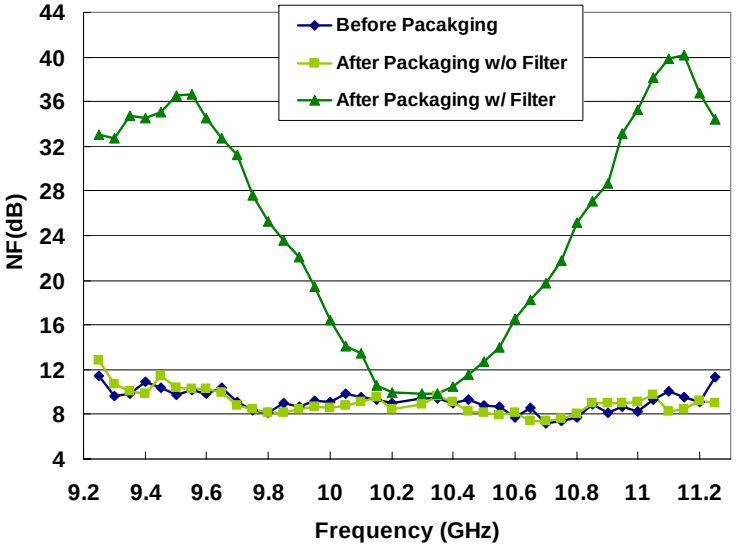
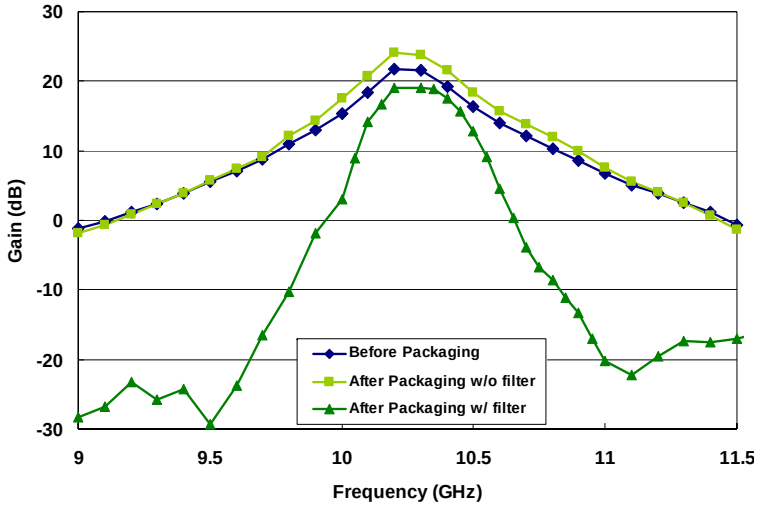
Measurement Results of 10GHz Package



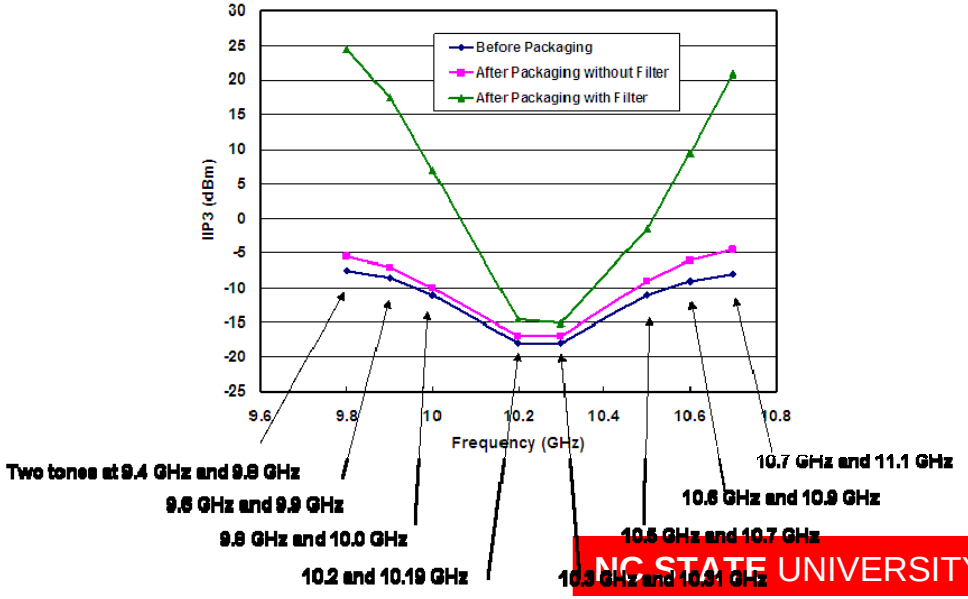
Noise Figure of IC and Package





Conversion Gains of IC and Package

Linearity of Packaged System



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Conclusion

- *Both Component and System Level Advantages were Demonstrated*
- *Components:*
  - *High-Q inductors/ transformers (Q's greater than 1000)*
  - *Filters (Q's greater than 1,000) and tunable*
  - *High-valued components*
- *System Demonstration*
  - *10 GHz Receiver Integrated at Wafer Scale*